KATHMANDU UNIVERSITY
End Semester Examination
February/March, 2019

Marks Scored:

Level : B.Sc.
Year : II

Course : PHYS 201
Semester: I

Exam Roll No. :

Time: 30 mins.

F. M. : 20

Registration No.:

Date 08 MAR 2019

SECTION "A"
[20Q. × 1 =20 marks]

Choose and tick the most appropriate answer. The symbols, unless mentioned otherwise, have their usual meanings.

1. Norton's theorem replaces a complicated circuit facing a load by an
   [a] ideal voltage source and parallel resistor.
   [b] ideal current source and parallel resistor.
   [c] ideal voltage source and series resistor.
   [d] ideal current source and series resistor.

2. The maximum power transfer to the load resistance R_L for the network of Figure A-1 is

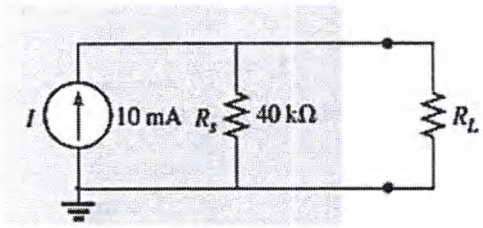

Figure A-1

[a] 1 W [b] $\frac{4}{10}$ W [c] 1 kW [d] $\frac{1}{5}$ W

3. An n-type semiconductor is a semiconductor that has been doped with
   [a] trivalent impurity atoms.
   [b] impurity atoms whose electron valence is +4.
   [c] pentavalent impurity atoms.
   [d] impurity atoms whose electron valence is +2.

4. If line frequency is 60 Hz, the output frequency of a bridge rectifier is
   [a] 30 Hz [b] 60 Hz [c] 120 Hz [d] 240 Hz

5. To display the digit 0 in a seven-segment indicator,
   [a] C must be off. [b] G must be off.
   [c] F must be on. [d] All segments must be lighted.

6. The base of an *npn* transistor is thin and
   [a] heavily doped. [b] lightly doped.
   [c] metallic. [d] doped by a pentavalent material.

7. In a class A amplifier, the collector current flows for
[a] less than half the cycle.
[b] half the cycle.
[c] less than the whole cycle
[d] the entire cycle.

8. The zener current for the loaded zener regulator shown in Figure A-2 is

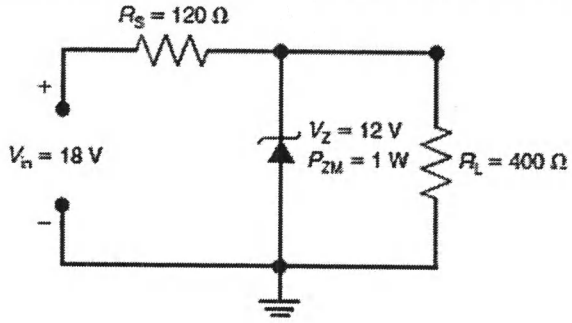

Figure A-2

[a] 50 mA [b] 40 mA [c] 30 mA [d] 20 mA

9. The silicon transistor in the base bias circuit shown in FigureA-3 has a β of 100. The equation of the dc load line is

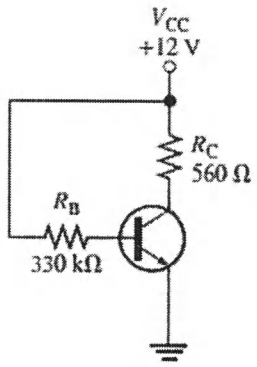

Figure A-3

[a] $I_C = -\frac{1}{100}V_{CE} + \frac{12}{100}$ [b] $I_C = \frac{1}{560}V_{CE} + \frac{12}{560}$

[c] $I_C = -\frac{1}{560}V_{CE} + \frac{12}{560}$ [d] $I_C = -\frac{1}{330}V_{CE} + \frac{12}{330}$

10. A depletion-type MOSFET is a
[a] normally off device. [b] normally on device.
[c] current-controlled device [d] bipolar device.

11. The input stage of every op amp is a
[a] differential amplifier. [b] push-pull amplifier.
[c] common base amplifier. [d] common emitter amplifier.

12. The Wien-bridge oscillator is useful
[a] at low frequencies. [b] at high frequencies.
[c] with LC tank circuits. [d] at small input signals.

13. The Hartley oscillator uses
[a] negative feedback. [b] two inductors.
[c] a tungsten lamp. [d] a tickler coil.

14. The binary equivalent of decimal 175 is
[a] 010 101 111 [b] 001 111 101 [c] 111 101 001 [d] 010 101 101

15. For the logic circuit shown in Figure A-4, which of the following Boolean statements gives the output Y in terms of inputs *A*, *B*, and *C?*

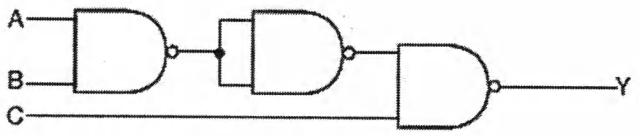

Figure A-4

[a] $Y=A \cdot B \cdot C$ [b] $Y=\overline{A \cdot B \cdot C}$ [c] $Y=\overline{A} \cdot \overline{B} \cdot \overline{C}$ [d] $Y=\overline{\overline{A \cdot B} \cdot C}$

Fill in the blank(s) with appropriate word(s) or value(s).

16. A circuit that adds a positive or negative dc voltage to an input sine-wave is called a ....

17. The all-important universal rule for biasing transistor for normal operation: The emitter-base junction must be ..... and the collector-base junction must be .....

18. The 2's complement representation of 1010 is .....

19. A certain op-amp has an open-loop voltage gain of 100,000 and a common-mode gain of 0.2. The CMMR is .....

20. When the values of I_{DSS} and $V_{GS(off)}$ are known for any JFET, the drain current, I_D, can be calculated using formula: .....

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SECTION "B"
[5Q. × 4 = 20 marks]

1. Define the dc alpha and dc beta of a transistor. Derive the equation $\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$.

2. Describe the proper polarities for (a) forward-biasing a diode, and (b) reverse-biasing a diode. Name the three diode approximations. What is the equivalent circuit for each of these approximations?

3. What is an oscillator? What are the conditions required for a circuit to oscillate? Draw the circuit diagram for the Colpitts oscillator and write the expression for its frequency of oscillation.

OR

Consider the circuit in Figure B-1.
Assume $R_1 = R_2 = R_3 = 10\text{k}\Omega$ and $C_1 = C_2 = C_3 = 0.001\mu\text{F}$
(a) Determine the value of R_f necessary for the circuit in Figure B-1 to operate as an oscillator.
(b) Determine the frequency of oscillation.

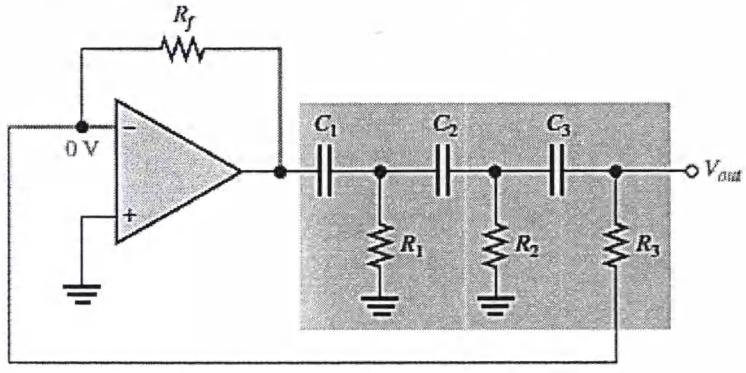

Figure B-1

4. What is the key difference in the way a JFET and MOSFET are constructed? Sketch the structure of an n-channel, enhancement-type MOSFET and explain their working.

5. The Macintosh computer processes binary numbers that are 32 bits long. If 32-bit number has all 1s, what is its decimal equivalent? Convert Hexadecimal C5E2 to a binary number.
Using 1's complemental method, subtract 01101_2 from 11011_2.

OR

Derive an accurate formula for the dc emitter current of a voltage-divider biased circuit.

SECTION "C"

[5Q. × 7= 35 marks]

6. Find the Thevenin equivalent circuit lying left to the terminals A-B in Figure C-1. What are the Norton equivalent values of I_N and R_N? Use Thevenin's theorem to calculate the load current in Figure C-1 for the following values of $R_L = 2\ \text{k}\Omega$ and $6\ \text{k}\Omega$.

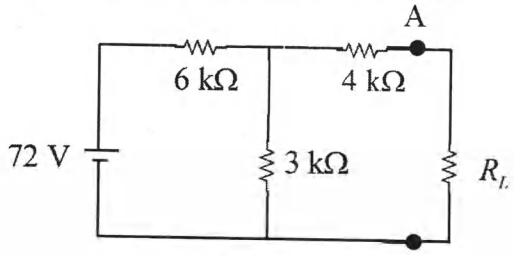

Figure C-1

7. Draw a circuit diagram for the CE amplifier as well as its dc and ac equivalent circuits. Derive the expression for the current gain, voltage gain, and power gain. Explain why there is phase inversion between input and output.

OR

Draw a circuit diagram for the RC-Coupled class A amplifier. Show that the maximum possible efficiency for any RC-Coupled class A amplifier is 8.33 percent.

8. What is the common-mode rejection ratio (CMMR) and how is it usually specified? Derive an expression for the closed-loop voltage gain of an inverting amplifier. Using inverting configuration of an op-amp, explain an op-amp differentiator.

9. State De Morgan's theorems. Explain the action of NAND gate with appropriate circuit diagram. Why NAND gate is called universal gate? Explain.

10. Distinguish between an avalanche and a Zener effects. Discuss Zener diode as a voltage regulator.

OR

Consider the circuit in Figure C-2.

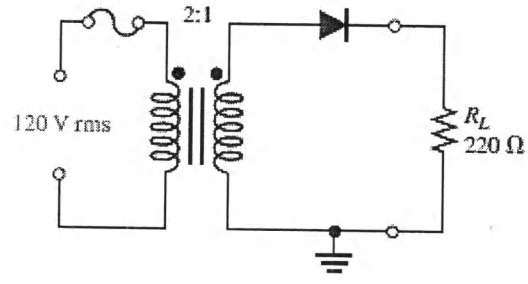

Figure C-2

(a) What type of circuit is this?
(b) Find the peak value of the secondary voltage.
(c) Sketch the voltage waveform across R_L.
(d) Find the dc load current for $R_L = 220\ \Omega$.
(e) What is the dc diode current?
(f) What is the PIV for diode?