KATHMANDU UNIVERSITY
End Semester Examination
March, 2022

Marks Scored:

Level : B.E.
Year : IV

Course : ETEG 431
Semester : II

Exam Roll No. :

Time : 30 mins.

F. M. : 10

Registration No.:

Date :

SECTION "A"

[20Q. × 0.5 = 10 marks]

Encircle the most appropriate option.

1. Which of the following logic families has the least power dissipation?
   a. RTL b. DTL c. CMOS d. ECL

2. Large scale integration circuits use
   a. TTL b. DL c. CMOS d. DTL

3. The NAND gate can function as a NOT gate if
   a. Inputs are connected together b. Inputs are left open
   c. One input is set to 0 d. One input is set to 1

4. When _____, toggle condition occurs in JK flip flop.
   a. J=0, K=1 b. J=0, K=0 c. J=1, K=0 d. J=1, K=1

5. Complete description of the circuit to be designed is given in _____.
   a. Architecture b. Entity c. Library d. Configurations

6. Which of the following is the correct use of the signal?
   a. To set a default value b. To pass value between circuits
   c. To declare a variable d. To represent local information

7. Multiple processes in a VHDL code are executed _____.
   a. Sequentially
   b. Randomly
   c. Based on the order of elements in the sensitivity list
   d. Concurrently

8. Which of the following type of memory is the fastest to access?
   a. ROM b. Cache c. SRAM d. DRAM

9. In _____ mapping, the data can be mapped anywhere in the Cache Memory.
   a. Associative b. Direct c. Set Associative d. Indirect

10. PAL stands for
a. Programmable Array Logic
b. Programmable Logic Array
c. Programmable Array Loaded
d. Programmable Adhoc Logic

11. Which of the following can be used for the area optimization of digital circuits?
a. Parallel structure
b. Retiming
c. Folding transformation
d. Replication

12. The ease with which the controller determines signal value at any node by setting input values is known as
a. Testability
b. Observability
c. Controllability
d. Manufacturability

13. Built-in self test
a. increases test pattern generation cost
b. reduces volume of test data
c. requires external ATE
d. increases test time

14. FPGA belongs to _____ devices.
a. SLD
b. SROM
c. EPROM
d. PLD

15. PLA contains _____.
a. AND and OR arrays
b. NAND and OR arrays
c. NOT and AND arrays
d. NOR and OR arrays

16. In an asynchronous sequential circuit, change in more than one state in response to a change in input is called
a. undefined condition
b. race condition
c. reset condition
d. ideal condition

17. Naming of the states is done in
a. transition table
b. stable state
c. flow table
d. excitation table

18. Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor?
a. Fan-out
b. Fan-in
c. Power dissipation
d. Propagation delay

19. The race in which stable state depends on an order is called
a. Critical race
b. Identical
c. Non critical race
d. Defined race

20. What do the Programmable Logic Devices (PLDs) designed especially for the combinational circuits comprise?
a. Only gates
b. Only flip flops
c. Gates and flip flops
d. Only memory devices

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SECTION "B"
[4Q. × 10 = 40 marks]

Attempt *ANY FOUR* questions. Symbols have their usual meanings. Urgent appropriate assumptions are permissible.

1.

a. Draw the circuit of NOR gate using CMOS and explain its operation. [5]
b. Discuss the basic characteristics of logic families. [5]

2.

a. What is the fundamental difference between the structural and behavioral design methodology? Implement the following Boolean expression using both structural and behavioral designs to illustrate such difference.
(A'+B).(C+D') [5]
b. Show how a PAL is programmed for the following 3-variable logic function.
Y=AB'C'+ABC+A'B'+BC [3]
c. Differentiate custom ICs and ASICs with examples. [2]

3.

a. Draw the logic circuit diagram of the SOP expression f=$\sum$ (2,3,6,7,11,12,13,15). Examine the possibility of hazards in the circuit. Explain how the hazard can be detected and eliminated with the aid of Karnaugh map. [5]
b. Give two valid differences between SRAM and DRAM. [2]
c. Discuss cache replacement policies in brief. [3]

4.

a. Discuss different strategies for area optimization while designing digital circuit. [5]
b. Lookup tables are used for implementing logic in Field-Programmable Gate Arrays (FPGAs). Explain with suitable example. [5]

5.

a. What are the differences between CPLD and FPGA? What are the advantages of FPGA? How is FPGA useful in the implementation of logic circuits? [5]
b. Explain briefly about various processes performed during testing of digital circuits. [3]
c. Define Stuck at fault model with example. [2]