Marks Scored :

KATHMANDU UNIVERSITY
End Semester Examination
March/April, 2017

APR 10 2017

Level : B. E.
Year : IV
Course : ETEG 431
Semester : I

Exam Roll No. :
Time: 30 mins.
F. M. : 10

Registration No.:
Date :

SECTION "A"
[20 Q. × 0.5= 10 marks]

Tick the most appropriate answer for each of the questions below.

1. _____ transistors in the pull-up network of a NOR gate are connected in _____.
[a] NMOS; parallel [b] NMOS; series [c] PMOS; parallel [d] PMOS; series

2. If MOS transistors of same size are used, speed of a 3-input CMOS gate would be _____ of that of an inverter.
[a] half [b] one-third [c] one-sixth [d] one-ninth

3. A 1-T DRAM cell stores its data in a _____.
[a] cross-coupled inverter [b] bit line
[c] capacitor [d] flip-flop

4. The threshold voltage of an EPROM transistor increases when the electrons are trapped in:
[a] drain [b] floating gate [c] channel [d] N-well

5. _____ memory architecture offers power saving capability.
[a] Hierarchal [b] Decoder-based [c] Array [d] Linear

6. FLASH memory can be regarded as a type of _____.
[a] SRAM [b] Hard-drive [c] EEPROM [d] CPLD

7. A PAL with M sum lines and N product lines can have _____ unique uncomplemented outputs.
[a] M [b] $\log_2(N)$ [c] $\log_2(M)$ [d] N

8. PLA and PROM both have _____ arrays.
[a] programmable OR [b] programmable AND
[c] fixed OR [d] fixed AND

9. Which of the following Verilog procedural block would most likely be inferred as an edge triggered logic with asynchronous reset?
[a] always @ (posedge clk and negedge rst) [b] always @ (posedge clk or postedge rst)
[c] always @ (clk_p or rst_n) [d] always @ (FDC)

10. If 'B' and 'C' are of 4 bits each, which of the following Verilog statements produces a result that is less than 4 bits in width?
[a] A = B + C;
[b] A = {B, C};
[c] A = {2{B}};
[d] A = &(B^C);

11. Which of the following is not a Verilog keyword?
[a] forever [b] always [c] repeat [d] again

12. The output of a three-input AND gate can be sensitized to a stuck-at fault at one of the inputs by holding the other two inputs at _____.
[a] 00 [b] 11 [c] 00 or 11 [d] 01 or 10

13. A fault-free NOR gate presented with a 'zero failing to one' (0 → 1) at one of its inputs can have either _____ or _____ at its output.
[a] 0 → 1; 1 → 0 [b] 1 → 0; 1 → 1 [c] 0 → 1; 0 → 0 [d] 1 → 0; 0 → 0

14. A static-0 hazard in _____ realization can be eliminated by using a redundant _____ gate.
[a] POS; OR [b] POS; AND [c] SOP; OR [d] SOP; AND

15. Which of the following techniques is used to reduce the area of a digital circuit?
[a] Structuring [b] H-tree [c] Parallelism [d] Flattening

16. In fundamental mode circuits, a race condition is non-critical if _____.
[a] there are two or more stable states in the destination column of the flow table
[b] there is only one stable state in the destination column of the flow table
[c] there is an unstable sate in between the two stable states
[d] there is a cycle in between the two stable states

17. Which among the following implementation options has the fastest time-to-market?
[a] ASIC [b] FPGA [c] Full Custom [d] Compiled Cell

18. Scan path improves the _____ of a sequential circuit.
[a] speed and area
[b] controllability and observability
[c] pipelining stages and parallel blocks
[d] fan-in and fan-out

19. Which of the following doesn't contribute to the hold time violations in flipflops?
[a] Setup time [b] Logic delay [c] C-to-Q time [d] Clock skew

20. Electromigration _____.
[a] decreases the reliability of a chip
[b] increases the life of a chip
[c] increases manufacturing defects in a chip
[d] decreases the area of a chip

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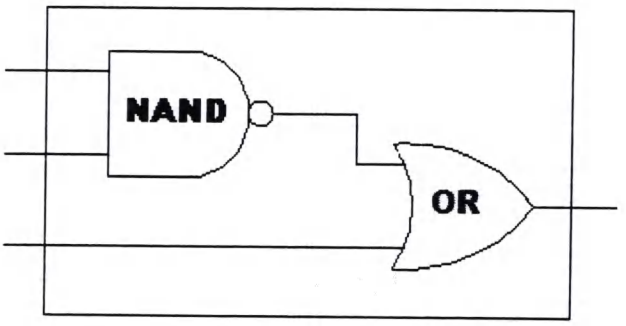
SECTION "B"

Attempt *ANY FIVE* questions. Missing data may be suitably assumed.

1. a. Construct a complex CMOS gate to realize the Boolean function, $f = \overline{A+B} \bullet \overline{CD}$. [3 + 1 + 4=8]
   b. Why are the CMOS gates with large number of inputs not desirable?
   c. Generate a minimal Fault Detection Test Set to cover all stuck-at faults in the circuit given below.



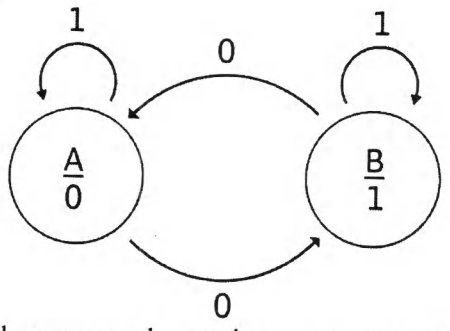
2. a. Distinguish between: [3 + 2 + 3=8]
      i. ASIC and Full-custom.
      ii. Gate Array and Standard Cell.
      iii. Programmable logic array and programmable logic sequencer.
   b. Implement the logic function, f(A,B,C) = AB + C in (i) PAL; (ii) PROM.
   c. What factors contribute towards the power dissipationof aCMOS circuit? What measures can be taken to reduce the power consumption of a CMOS circuit?

3. a. Explain the working of 1-T DRAM with the help of suitable diagram. Compare it with 6-T SRAM. [3 + 3 + 2=8]
   b. Discuss the use of Floating gate transistors in different types of nonvolatile semiconductor memories.
   c. Describe Array memory architecture.

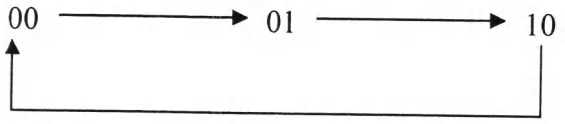
4. a. Distinguish between 'reg' and 'wire' Verilog data types. [1 + 2 + 5=8]
   b. Rewrite the following Verilog module to minimize the chip area.

```
moduleeteg (  input [3:0] a,
              input [3:0] b,
              input  [3:0] c,
              inputsel
              output wire [7:0] result);
wire [7:0] res_a;
wire [7:0] res_b;

assign result = sel?res_a :res_b;
assignres_a = a * c;
assignres_b = b * c;

endmodule
```

   c. Write a Verilog module to implement the following state diagram. Also, write a Verilog testbench for the module.



5. a. Distinguish between synchronous and asynchronous sequential circuits. [1 + 2 + 5=8]
   b. Redesign the circuit, $f = A\bar{B} + B\bar{C}$ such that the circuit does not produce a static hazard when there is a change in a single input.
   c. Design a Fundamental mode asynchronous sequential circuit, with one-bit input, that produces the following two-bit output sequence:



where, arrow (→) indicates a change in input. Avoid critical race.

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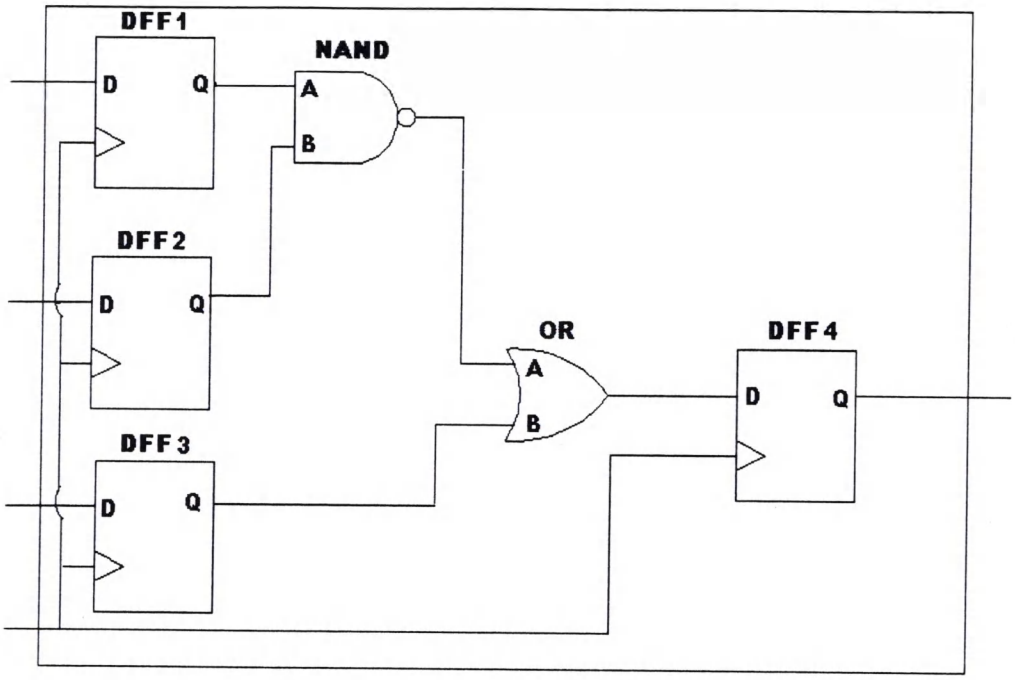
6. a. Construct a JK-flipflop with active high asynchronous reset using CMOS pass switches. [3 + 1 + 4=8]

   b. Why does a CMOS gate have different slew rates?

   c. Consider the circuit given below. Clock skew is 0.004ns. Setup time and hold time for the flipflops are 0.007ns and 0.008ns respectively. Delay in the wires is negligible. Other parameters are given in the table below. Determine the maximum clock frequencyof the circuit. Also, check the circuit for hold time violation.



DATA

NAND

Input Load:

Pin Name	Load (fF)
A	3.2
B	3.4

Slew Factor:

Factor (ns/fF)	0.03
Constant (ns)	0.05

OR

Input Load:

Pin Name	Load (fF)
A	3.5
B	3.8

Slew Factor:

Factor (ns/fF)	0.04
Constant (ns)	0.06

DFF

Input Load:

Pin Name	Load (fF)
D	2.9

Slew Factor:

Factor (ns/fF)	0.02
Constant (ns)	0.04