KATHMANDU UNIVERSITY
End Semester Examination
June/July, 2023

Marks scored:

Level : B.E.
Year : III
Course : EEEG 320
Semester : II

Exam Roll No. :
Time: 30 mins.
F. M. : 10

Registration No.:
Date 29 JUN 2023

SECTION "A"
[20Q. × 0.5 = 10 marks]

Encircle the most appropriate option. Symbols have their usual meaning.

1. In the TTL Family, HIGH output corresponds to _____.
   a. 2.4V to 5V b. 2V to 5V c. 0.8 V to 2 V d. 0.4 V to 2.4 V

2. Which of the following logic families has the highest speed?
   a. RTL b. DTL c. CMOS d. ECL

3. Karnaugh map is used to _____.
   a. minimize the number of flip-flop in a digital circuits
   b. to design gates
   c. to minimize the number of gates in only a digital circuit
   d. to minimize the number of gates and fan-in requirements of the gates in a digital circuit

4. Race around condition occurs in a J-K flip-flop when_____.
   a. both the inputs are 0 b. both the inputs are 1
   c. the inputs are complementary d. any combination of inputs

5. Which of the following signal cause the process to execute?

```
PROCESS(clr)
BEGIN
IF (clr= '1') THEN
y <= '0';
ELSE
y<= input;
END PROCESS;
```

   a. input b. y c. clr d. clk

6. Refer to the code given below, what kind of circuit is designed?

```
SIGNAL x : IN BIT;
SIGNAL y : OUT BIT;
SIGNAL clk : IN BIT;
PROCESS (clk)
BEGIN
IF (clk'EVENT and clk = '1')
y <= x;
END PROCESS
```

   a. Buffer b. Latch c. Flip-Flop d. Shift Register

7. To reduce memory access time, a small, fast memory is inserted between the main memory and the processor. What is this memory called?
a. Accumulator b. Register c. Dynamic RAM d. Cache

8. If a and b are two STD_LOGIC_VECTOR input signals, then legal assignment for a and b is _____?
a. x < a.b b. x<= a OR b c. x<= a + b d. x <= a && b

9. Reduction in power dissipation can be brought by_____.
a. increasing transistor area b. decreasing transistor area
c. increasing transistor feature size d. decreasing transistor feature size

10. Large scale integration circuits use _____.
a. TTL b. DL c. CMOS d. DTL

11. FPGA device are _____ type.
a. PLD b. EPROM c. SROM d. SLD

12. Which of the following is true in case of Mealy machine?
a. Output is same as state b. Output is function of input and state
c. Output is function of inputs d. Output is function of states

13. PLDs with programmable AND and fixed OR arrays are called _____.
a. PAL b. PLA c. APL d. PPL

14. ASIC stands for _____.
a. American Specific Instruction Code
b. Application Specific Integrated Circuits
c. Application specific Instruction Code
d. American Standard Instruction Code

15. Which of the following memory must be refreshed many times per second?
a. EPROM b. ROM c. Static RAM d. Dynamic RAM

16. Which of the following mode of the signal is bidirectional?
a. IN b. OUT c. INOUT d. BUFFER

17. What does the architecture of an entity define?
a. External interface b. Internal functionality
c. Ports of the entity d. Specifications

18. A 7-input AND gate has a fan in of _____.
a. 1 b. 2 c. 7 d. 8

19. In the asynchronous circuit, the changes occur with the change of _____.
a. Input b. output c. clock pulse d. time

20. The circuit should be tested at _____.
a. design level b. chip level c. transistor level d. switch level

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Time : 2 hrs. 30 mins.

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Semester : II
F.M. : 40

SECTON "B"
[4Q. × 10 = 40 marks]

Attempt *ANY FOUR* questions. Symbols have their usual meanings. Urgent appropriate assumptions are permissible.

1. a. What are the steps to design combinational circuits? Implement OR and EX-OR gates using only NAND gates. [2+3]

   b. Discuss the basic characteristics of logic families. Implement NAND gates using CMOS. [3+2]

2. a. Draw the logic circuit diagram of the SOP expression f= ∑(2,3,6,7,11,12,13,15). Examine the possibility of hazards in the circuit. Explain how the hazard can be detected and eliminated with the aid of Karnaugh map. [5]

   b. Discuss one of the strategy for improving timing of a digital circuit design in brief. Explain with an example. [5]

3. a. Consider thefollowing VHDL code:

```
demo_process: process(A,B)
begin
if B='1'then A<= 0;
else A<=1;
C <= A and B;
end process demo_process;
```

   Suppose when this process is executed, the current values of A and B are both 1. After this process finishes, what will be the value of C? [3]

   b. What are the different cache replacement policies? Explain each in brief. [5]

   c. Differentiate between fundamental and pulse mode asynchronous sequential circuits. [2]

4. a. Write a VHDL code for a single traffic light controller. Assume you have 60 Hz clock signal. Your design should allow asynchronous reset. When the circuit is reset, the traffic light should be RED. The waiting times are as follows: Red (50 sec), Yellow (10 sec), and Green (55 sec). [5]

   b. Design a combinational circuit using a ROM such that the circuit accepts 3-bit number and generate an output binary number equal to the square of the input numbers. [5]

5. a. List the characteristics of FPGA. [2]

   b. Explain critical and non-critical races in asynchronous sequential circuits with the aid of an appropriate state transition table. [4]

   c. Explain the basic testing principle of digital circuits. Briefly explain the architecture of Built In Self-Test (BIST)? [2+2]