KATHMANDU UNIVERSITY
End Semester Examination
July/August, 2024

Marks Scored:

Level : B.E.
Year : III

Course : EEEG 320
Semester : II

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date 30 JUL 2024

SECTION "A"

[20 Q. × 0.5 = 10 marks]

Choose and encircle in the most appropriate option from each set of choices

1. How many bits are needed to store one BCD digit?
   a. 2 bits b. 4 bits c. 3 bits d. 1 bit

2. Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption?
   a. PMOS b. NMOS c. CMOS d. ECL

3. Transistor–transistor logic (TTL) is a class of digital circuits built from _____ .
   a. JFET only
   b. Bipolar junction transistors (BJT)
   c. Resistors
   d. Bipolar junction transistors (BJT) and resistors

4. Latches are called memory devices because
   a. It has capability to stare 8 bits of data b. It has internal memory of 4 bit
   c. It can store one bit of data d. It can store infinite amount of data

5. In VHDL, which object/s is/are used to connect entities together for the model formation?
   a. Constant b. Variable c. Signal d. entity

6. In VHDL, complete description of the circuit to be designed is given in _____.
   a. Architecture b. Entity c. Library d. Configurations

7. _____ is a chip by which both the operation of read and write is performed.
   a. RAM b. ROM c. PROM d. EPROM

8. Whenever the data is found in the cache memory, it is called as _____.
   a. HIT b. MISS c. FOUND d. ERROR

9. Asynchronous sequential logic circuit does not use
   a. inputs b. outputs c. clock pulses d. time

10. Race condition is present in
    a. synchronous logic circuit b. asynchronous logic circuit
    c. ideal logic circuit d. combinational logic circuits

11. Programmable logic array has
    a. Fixed OR plane followed by a programmable AND gate
    b. Fixed AND plane followed by a programmable OR gate
    c. Programmable OR gate followed by a fixed AND gate
    d. Programmable AND gate followed by a programmable OR gate

12. Vertical and horizontal directions in FPGA are separated by_____ .
    a. A channel b. A line c. A flip-flop d. A strobe

13. What is the maximum noise voltage that may appear at the input of a logic gate without changing the logical state of its output is termed as _____
    a. Noise Immunity b. Noise Margin c. White Noise d. Gaussian Noise

14. Most look-up tables in field-programmable gate arrays (FGPAs) use _____ inputs, resulting in _____ possible outputs.
    a. 4,16 b. 8,16 c. 4,12 d. 6,12

15. Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?
    a. Simulation b. Optimization c. Synthesis d. Verification

16. Medium scale integration has _____.
    a. ten logic gates b. fifty logic gates
    c. hundred logic gates d. thousands logic gates

17. The race in which stable state is independent of order is called _____.
    a. critical race b. identical race c. non critical race d. defined race

18. The purpose of Design for Test (DFT) process in ASIC design is
    a. To capture functional errors b. To capture manufacturing defects
    c. To capture timing violations d. To mitigate radiation

19. Adding extra register layer while designing digital systems improves
    a. timing b. area c. power d. testing

20. Built-in self-test (BIST) does not aim to
    a. reduce test pattern generation cost b. reduce volume of test data
    c. reduce test time d. reduce area

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SECTION "B"
[4 Q. × 10 = 40 marks]

Attempt *ANY FOUR* questions. *Symbols have their usual meanings. Urgent appropriate assumptions are permissible. Marks are indicated inside brackets.*

1.
   a. Draw a logic diagram that implements the expression A(B+C)(C'+D)(B+D') directly using only simple gates. Simplify the expression and draw simplified the logic diagram. [2+2]
   b. Compare the characteristics of RTL, TTL, ECL and CMOS logic families. Explain analytically the behavior of a CMOS inverter with its diagram. [2+2]
   c. Design a hazard free circuit for $F(X,Y,Z) = \sum(3,4,6,7)$. [2]

2.
   a. Mention the types of hazard that occur in combinational circuits. Demonstrate the occurrence of static 0-hazard with a suitable example and the methods to eliminate hazards in combinational circuits. [1+3]
   b. List different strategies for improving timing while designing digital circuit. Explain any one of them. [1+3]
   c. Write a VHDL code for a 2 bit magnitude comparator. [2]

3.
   a. Write a VHDL code and test bench for a 3 to 8 decoder implemented using basic logic gates such as AND, OR etc.. The entity port has one 3-bit input and one 8-bit decoded output. [2+3]
   b. Discuss different types of ASICs in brief. [3]
   c. Discuss cache replacement policies in brief. [2]

4.
   a. Explain the mapping of a 2x4 decoder to 3-input 2-output LUTs in FPGA with an example. [4]
   b. Show how a PLA is programmed for the following 3-variable logic function. [4]
      $F_1 = B'C' + A'C$ and
      $F_2 = A'B + A'C + AB'$.
   c. Differentiate between synchronous and asynchronous sequential circuits. [2]

5.
   a. How does the PLDs differ from fixed logic devices? Draw the basic FPGA architecture. [3]
   b. An asynchronous sequential circuit is described by the following excitation and output function,
      $Y = xy_1 + x'y_2$
      $Z = xy_1' + x'y_2$
      i. Draw the logic diagram of the circuit.
      ii. Derive the transition table, flow table and output map. [1+3]
   c. Describe the architecture of Built in self-test (BIST). Discuss common fault models in digital system design. [3]