KATHMANDU UNIVERSITY
End Semester Examination
February, 2025

Marks Scored:

Level : B.E.
Year : III

Course : EEEG 320
Semester : II

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date 14 FEB 2025

SECTION "A"

[20 Q. × 0.5 = 10 marks]

Choose and encircle the most appropriate option from each set of choices

1. Don't care conditions can be used for simplifying Boolean expressions in _____
   a. Registers b. Terms c. K-maps d. Latches

2. Half-adders have a major limitation in that they cannot _____
   a. Accept a carry bit from a present stage
   b. Accept a carry bit from a next stage
   c. Accept a carry bit from a previous stage
   d. Accept a carry bit from the following stages

3. How many outputs will a decimal-to-BCD encoder have?
   a. 4 b. 8 c. 12 d. 16

4. In a stable logic state TTL devices consume substantially _____ power than equivalent CMOS.
   a. less b. more c. equal d. very high

5. Which of the following is not the advantage of MOS gates?
   a. Low power dissipation b. Small size
   c. Good immunity to noise d. High switching speeds

6. Which of the following VHDL design units contain the description of the circuit?
   a. Configurations b. Architecture c. Library d. Entity

7. How many times will this process print "EEEG 320"?

```
process is
begin
        report "EEEG 320";
        wait for 10 ns;
end process;
```

   a. Only one time b. Always 11 times
   c. Always 10 times d. Depends on for how long we simulate

8. In VHDL, which keyword is used to specify ports?
   a. Port_name b. Value_port c. Port d. Pt

9. Which of the following memories must be refreshed many times per second?
   a. Static RAM b. Dynamic RAM c. ROM d. EPROM

10. ROM is made up of _____
a. NAND and OR gates
b. NOR and decoder
c. Decoder and OR gates
d. NAND and decoder

11. If the output is currently at logic state 1 and after the input changes its state, the output momentarily changes to 0 before settling on 1, then it is a
a. Static-1 hazard
b. Static-0 hazard
c. Dynamic hazard
d. Functional hazard

12. A Condition occurs when an Asynchronous sequential circuit changes two or more binary states variables is known as
a. deadlock condition
b. Running condition
c. Race condition
d. Livelock

13. What does ASIC stand for in the context of integrated circuits?
a. Automated System Integration Circuit
b. Advanced System Integrated Circuit
c. Analog Signal Integrated Circuit
d. Application Specific Integrated Circuit

14. What is the main disadvantage of a Full Custom ASIC design approach?
a. Easy and quick design process
b. Limited customization options
c. Low performance output
d. High design time, complexity, and cost

15. PLAs, CPLDs, and FPGAs are all which type of device?
a. SLD
b. PLD
c. EPROM
d. SRAM

16. A ROM of size M x N bits can store
a. N words of M bits each
b. M words of N bits each
c. M bits
d. N bits

17. For the PAL design of a logic circuit, a single literal term
a. requires an AND gate
b. does not require an AND gate
c. requires an AND gate and one input for OR gate
d. requires an inverter

18. The major difficulty in sequential circuit testing is in
a. determining output
b. determining internal state
c. determining external state
d. determining input combinations

19. The critical path is the path between
a. Two combinational circuits
b. Two sequential circuits
c. Two decoders
d. Two multiplexers

20. _____ is not a strategy to improve timing of a digital circuit design.
a. Add register layer
b. Parallel structure
c. Folding
d. Retiming

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Level : B.E.
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Time : 2 hrs. 30mins.

14 FEB 2025

Course : EEEG 320
Semester : II
F. M. : 40

SECTION "B"
[4 Q. × 10 = 40 marks]

Attempt ANY FOUR questions. Each question carries 10 marks. Symbols have their usual meanings. Urgent appropriate assumptions are permissible. Marks are indicated inside brackets.

1.

a. Differentiate Mealy and Moore sequential circuits. [3]
b. ompare the characteristics of TTL and CMOS logic families. Explain analytically the behavior of a CMOS based NAND gate with its diagram. [2+2]
c. Realize the Boolean function $F(X,Y,Z)=\sum(1,3,4,5)$ using logic gates for hazard free. [3]

2.

a. What is the advantage of using PLDs in the design of digital systems? Discuss static hazards in digital circuits with examples. [1+2]
b. An asynchronous sequential circuit is described by the following excitation and output and output function,
$Y_1= X_1X_2+X_1Y_2+X_2Y_1$
$Y_2=X_2+X_1Y_1Y_2+X_1Y_1$
$Z= X_2+Y_1$
i) Draw the logic diagram of the circuit.
ii) Derive the transition table and output map. [4]
c. Explain the concept of "entity" and "architecture" in VHDL. State the difference between signal and a variable in VHDL. [2+1]

3.

a. Design a logic diagram for a gray to binary conversion. Write a VHDL code for the gray to binary conversion. [3+3]
b. Differentiate between custom ICs and ASICs. [2]
c. Discuss fully associative cache mapping techniques in brief. [2]

4.

a. Explain system partitioning and routing in FPGA design flow. [3]
b. Design following functions using PLA.
$Y_1= AB + AC'+AB'$
$Y_2=AB+A'C+AC$ [4]
c. List the advantages and disadvantages of asynchronous sequential circuit. [3]

5.

a. Explain an architecture of FPGA with a diagram. [3]
b. What are the different levels at which testing is carried out? Differentiate between delay fault model and bridging fault model. [2+2]
c. Explain how folding and resource sharing helps to optimize area while designing digital circuit. [3]