KATHMANDU UNIVERSITY
End Semester Examination [C]
November/December, 2023

Marks scored:

Level : B.E.
Year : III
Course : EEEG 320
Semester : II

Exam Roll No. :
Time: 30 mins.
F. M. : 10

Registration No.:
Date 05 DEC 2023

SECTION "A"
[20Q. × 0.5 = 10 marks]

Encircle the most appropriate option. Symbols have their usual meaning.

1. A digital circuit that can store only one bit is a _____
   c. Register b. NOR gate c. Flip-flop d. XOR gate

2. TTL stands for _____.
   a. Transistor-Transistor Logic b. Transistor-Thermocouple Logic
   c. Transistor-Thermostat Logic d. Transistor-Thermistor Logic

3. Which of the following logic families has the lowest power consumption?
   a. RTL b. DTL c. CMOS d. ECL

4. K- map for full adder is of _____ variable(s).
   a. 2 b. 3 c. 4 d. 1

5. How many input and output are needed for de-multiplexer?
   a. Many outputs to one input b. One input many outputs
   c. one input one output d. Many inputs many outputs

6. Using VHDL ____, one can transfer data between components or inside them.
   a. Package b. Port c. Signal d. Component

7. In VHDL, variables are assigned using which of the following?
   c. ::< b. =< c. <= d. :<

8. The most basic form of behavioral modeling in VHDL is _____.
   a. If statements b. Assignment statements
   c. Loop statements d. WAIT statements

9. The table that is not a part of the asynchronous analysis procedure is
   a. Transition table b. State table
   b. Flow table d. Excitation table

10. The race in which stable state depends on an order is called _____.
    a. critical race b. identical race
    c. non critical race d. defined race

11. Naming the states is done in
    a. Transition table
    b. stable state
    c. flow table
    d. excitation table

12. FPGA device are _____ type.
    a. PLD
    b. EPROM
    c. SROM
    d. SLD

13. Programmable Logic Arrays contains _____ .
    a. AND and OR arrays
    b. NAND and OR arrays
    c. NOT and AND arrays
    d. NOR and OR arrays

14. Most FPGA logic modules utilize a(n) _____ approach to create the desired logic functions.
    a. AND array
    b. Look-up table
    c. OR array
    d. AND and OR array

15. Which flip-flop is usually used in the implementation of the registers?
    a. D flip-flop
    b. S-R flip-flop
    c. T flip-flop
    d. J-K flip-flop

16. Which is the fastest cache mapping function?
    a. Random mapping
    b. Set associative mapping
    c. Fully associative mapping
    d. Direct Mapping

17. The address bus with a ROM of size 1024 × 8 bits is _____
    a. 8 bits
    b. 12 bits
    c. 10 bits
    d. 16 bits

18. The output of the logic synthesis phase in ASIC flow is usually represented in
    a. C programming language
    b. RTL
    c. Verilog or VHDL
    d. Assembly language

19. Leakage power is inversely proportional to _____ .
    a. Frequency
    b. Load capacitance
    c. Supply voltage
    d. Threshold voltage

20. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____ .
    a. Level 1 cache
    b. Level 2 cache
    c. Registers
    d. TLB

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Level : B.E.
Year : III
Time : 2 hrs. 30 mins.

Course : EEEG 320
Semester : II
F.M. : 40

SECTON "B"
[4Q. × 10 = 40 marks]

Attempt *ANY FOUR* questions. Symbols have their usual meanings. Urgent appropriate assumptions are permissible.

1. a. What are the steps to design sequential circuits? Implement OR and EX-OR gates using only NOR gates. [3+2]

   b. Differentiate Mealy and Moore sequential circuits. Implement NOR gates using CMOS. [3+2]

2. a. Draw the logic circuit diagram of the SOP expression
   $F(A,B,C,D)= \sum(0,2,5,6,7,8,9,12,13,15)$.
   Examine the possibility of hazards in the circuit. Explain how the hazard can be detected and eliminated with the aid of Karnaugh map. [5]

   b. Discuss different strategies for area optimization while designing digital circuit. [5]

3. a. Consider the following VHDL code, answer the following. [3]

```
ENTITY simple IS PORT(
        a,b,c: IN std_logic;
        x: OUT std_logic;
END SIMPLE;

ARCHITECTURE are OF simple IS
BEGIN
        X<=(a OR (b AND NOT c));
END are;
```

   i. How many inputs are there and what type?
   ii. How many outputs are there and what type?
   iii. Draw the logic circuits schematic that is equivalent to the VHDL code.

   b. What are cache memory mapping techniques? Explain each in brief. [4]

   c. Give three valid differences between SRAM and DRAM. [3]

4. a. It is required to design a majority logic circuit whose output is equal to 1 if the majority of the inputs are 1's. The output is 0 otherwise. The circuit has 3 inputs and it produces logic one if more than one of its inputs are logic one. [5]
   i. Draw the schematic diagram of the circuit using only NAND gates.
   ii. Write the VHDL code for the previous circuit using structural approach (you have to define NAND gate in VHDL first).

   b. Show how a PAL is programmed for the following 3-variable logic function.
   Y=AB'C'+ABC+A'B'+BC [5]

5. a. Differentiate FPGA and CPLDs. [2]

   b. An asynchronous sequential circuit is described by the following excitation and output function, [4]
   $Y = x_1 x_2 + (x_1 + x_2)\, y$
   $Z = Y$
   i. Draw the logic diagram of the circuit.
   ii. Derive the transition table, flow table and output map.
   iii. Describe the behavior of the circuit. Explain critical and non-critical races in asynchronous sequential circuits with the aid of an appropriate state transition table.

   c. What is the basic objective of circuit testing? Discuss various processes during testing in brief. [2+2]