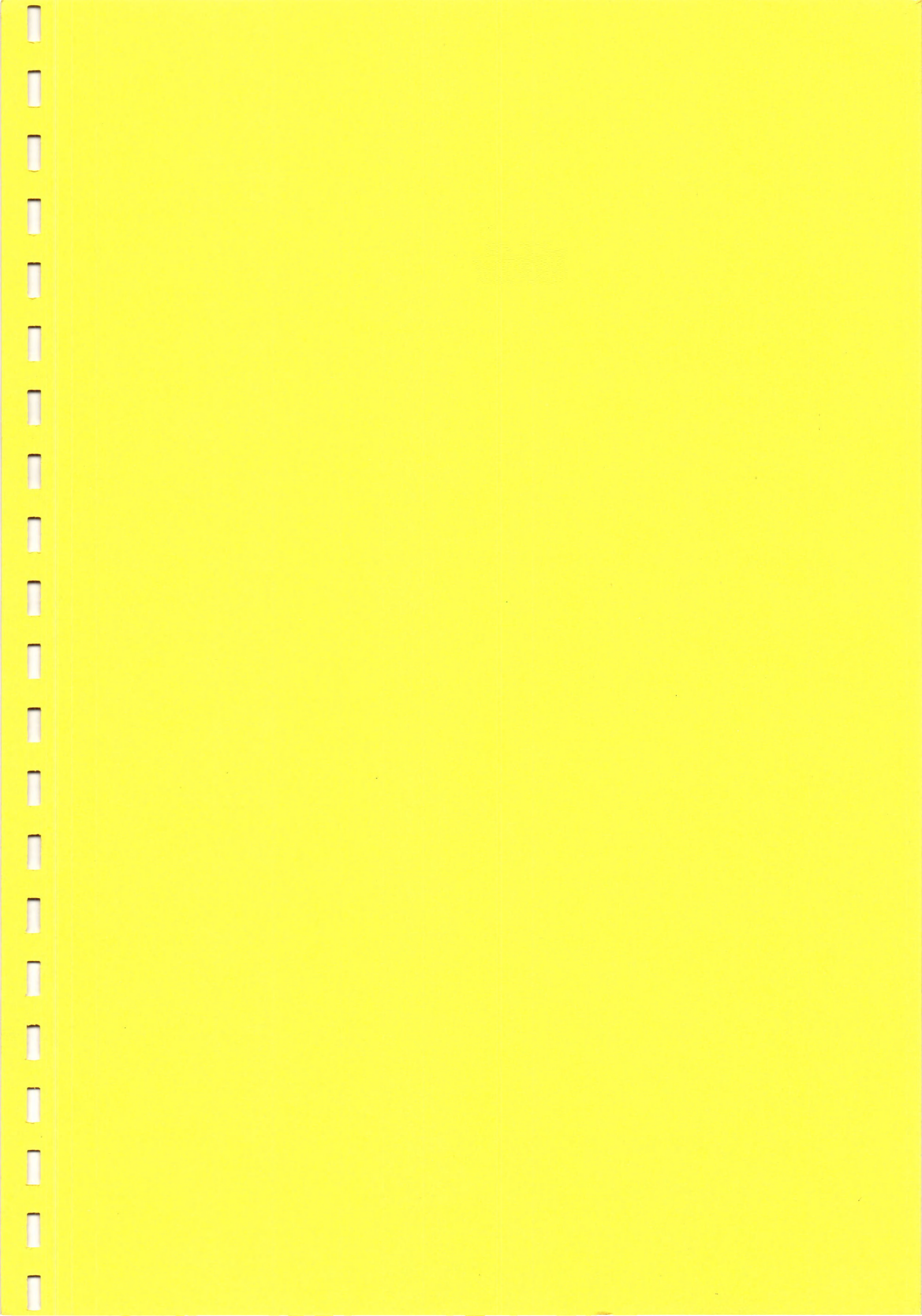


KATHMANDU UNIVERSITY
End Semester Examination [C]
May/June, 2019

Marks Scored:

Level : B.E.
Year : III

Course : EEG 314
Semester: I



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End Semester Examination [C]
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Exam Roll No.:

Time: 30 mins.

F.M. : 20

Registration No.:

Date 09 JUN 2019

SECTION "A"
[20Q. × 1 = 20 marks]

Encircle the most appropriate answer among the given options.

1. _____ is the basic steps of execution of an instruction.
a. Fetch → Decode → Execute b. Decode → Fetch → Execute
c. Fetch → Execute → Decode d. Execute → Fetch → Decode
2. _____ Interrupt is not a vectored interrupt.
a. INTR b. TRAP c. RST 7.5 d. RST 3
3. NMI is a _____ interrupt.
a. Type 0 b. Type 1 c. Type 2 d. Type 3
4. Output of the assembler in machine codes is referred to as _____.
a. Object Program b. Source Program c. Macro instruction d. Symbolic Addressing
5. SIM stands for _____.
a. Select Interrupt Mask b. Set Interrupt Mask
c. Sort Interrupt Mask d. Sum Interrupt Mask
6. Address line for RST3 is _____.
a. 0020H b. 0028H c. 0018H d. 0010H
7. _____ Interrupt has the highest priority.
a. INTR b. TRAP c. RST 6.5 d. RST7.5
8. _____ are the two major components of CPU?
a. CU/registers b. Registers/Memory c. CU/ALU d. ALU/Bus
9. Data storage in stack is designed in _____ method.
a. FIFO b. LILO c. FILO d. LIFO
10. The language that the computer can understand and execute is _____ language.
a. Object b. HEX c. System d. Machine
11. Registers used to hold condition are called _____.
a. PC b. Memory address c. Accumulator d. Flags
12. PSW has _____ five flags
a. S,Z,AC,P,CY b. S, OV, AC, P, CY c. S,Z,OV,P,CY d. S,Z,AC,P,OV
13. The _____ cycle is required to fetch and execute instruction in 8085 microprocessor.
a. clock b. memory c. machine d. instruction

14. _____ is the instruction that avoids unnecessary Jumps to terminate the program.
a. HLT b. NOP c. RET d. EI
15. The address/data bus in 8085 is _____.
a. multiplexed b. demultiplexed c. encoded d. decoded
16. _____ Memory types cannot be re-written after once.
a. PROM b. EPROM c. EEPROM d. EAROM
17. In 8085 ALE signal is made high to _____.
a. To latch lower address from data bus
b. To disable data bus
c. To write in data bus
d. Enable data bus to be used as address bus
18. _____ does not belong to 8085 flag register.
a. Carry Flag b. Sign Flag c. Zero Flag d. One Flag
19. _____ Instruction sets the carry flag.
a. CY set b. STR c. STC d. Set CY
20. The _____ chip is a latch.
a. 74LS138 b. 74LS373 c. 74LS244 d. 74LS245

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Semester: I
F.M. : 55

SECTION "B"

- ✓ Attempt any FIVE questions
- ✓ Assume any suitable data if necessary
- ✓ Figures in margin indicate full marks for each questions

1.

- a) Explain briefly the architecture of 8085 microprocessor. [4]
- b) How can the lower address $AD_0 - AD_7$ demultiplexed in 8085. Explain with suitable diagram. [3]
- c) Write a program to shift an eight bit data four bits right. Assume that data is in register C. [4]

2.

- a) Design an interfacing circuit for input and output devices using a decoder with input address FAH and output address F8H. [4]
- b) The memory map of a 4K (4096) byte memory chip begins at the location 2000H. Specify the address of the last location on the chip and the number of pages in the chip. [3]
- c) Explain various machine cycles in 8085 with examples. [4]

3.

- a) Design a counter with 5 s delay using register pair. Assume frequency = 1MHz. Show the calculations clearly. [4]
- b) Explain the differences between CALL/RET and PUSH/POP. [3]
- c) Write the process to clear all the flags and demonstrate whether the zero flag is affected by data transfer operation or not using PUSH and POP operations. [4]

4.

- a) Explain operation of interfacing an 8-bit A/D converter using a status check. [4]
- b) Specify the handshake signals for port A of the 8155 if the port A is connected as an input port in the interrupt mode. Explain the sequence of events and timing in data input. [4]
- c) What are different types of logic operations in 8085? Explain their operation. [3]

5.

- a) What are the various operations performed by a microprocessor. [4]
- b) Draw a block diagram of Microprocessor Controlled Temperature System and explain the components used. [5]
- c) Calculate the values of LSB, MSB and full-scale output for an 8-bit DAC for the 0V to 10V range. [2]

6.

- a) Write short notes on [2 × 3 = 6]
 - i. Interrupts
 - ii. Digital to Analog Converter
 - iii. Memory Interfacing
- b) A block of data is stored in the memory locations from XX55H to XX5AH. Transfer the data to the locations XX80H to XX85H in the reverse order.
Data: 22, A5, B2, 99, 7F, 37 [5]

