

KATHMANDU UNIVERSITY  
End Semester Examination  
July/August, 2024

Marks Scored:

Level : B.E.

Year : III

Exam Roll No. :

Time: 30 mins.

Registration No.:

Course : EEEG 314

Semester : I

F. M. : 10

Date : 05 AUG 2024

SECTION "A"

[20 Q. × 0.5 = 10 marks]

Choose and encircle in the most appropriate option from each set of choices

- You are designing a multi-core processor where each core follows RISC principles. To maximize the performance of parallel processing, which of the following strategies should you avoid?
  - Ensuring that each core can independently fetch and decode instructions.
  - Sharing a common cache for frequently accessed data among all cores.
  - Designing complex instructions that each core can execute independently.
  - Implementing efficient inter-core communication mechanisms.
- Considering the Intel 8085 microprocessor, which of the following instructions requires the least number of clock cycles to execute?
  - MOV A, B
  - ADD M
  - CALL 2000H
  - LXI H, 2050H
- In the context of the Intel 8085 microprocessor, what will be the status of the Zero (Z) flag after executing the following instructions?  
MVI A, 00H  
ANI 00H
  - Z flag will be set to 0.
  - Z flag will be set to 1.
  - Z flag will remain unchanged.
  - Z flag will be in an undefined state.
- Which of the following operations would take the longest time to complete in the Intel 8086 microprocessor, assuming all instructions are executed sequentially and without any interruptions?
  - MOV AX, BX
  - DIV BX
  - ADD AX, BX
  - JMP 1234H
- Given the instruction MOV AX, [BX+SI] in the Intel 8086, what type of addressing mode is being used?
  - Immediate addressing
  - Direct addressing
  - Register indirect addressing
  - Base-index addressing
- The BIU pre-fetches the instruction from memory and store them in \_\_\_\_\_.
  - register
  - queue
  - memory
  - stack
- Address line for RST3 is \_\_\_\_\_.
  - 0020H
  - 0028H
  - 0018H
  - 0010H
- \_\_\_\_\_ are level triggering interrupts.
  - INTR & TRAP
  - RST 6.5 & RST 5.5
  - RST 7.5 & RST 6.5
  - RST
- In 8085, multiplexed address bus and data bus are separated via \_\_\_\_\_ signal.
  - IO/MR
  - DMA
  - ALE
  - INTR



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Level : B.E.  
Year : III  
Time : 2 hrs. 30mins.

Course : EEEG 314  
Semester : I  
F. M. : 40

05 AUG 2024

SECTION "B"

[4 Q. × 10 = 40 marks]

*Attempt ANY FOUR questions. Assume any suitable data if necessary. Figures in margin indicate full marks for each questions*

1.
  - a. Why demultiplexing the bus  $AD_7 - AD_0$  is needed and how it is done in 8085? [2]
  - b. Draw and explain the timing diagram for STA 8085H instruction. [4]
  - c. Write a program to find the largest number stored from memory location 4000H to 4009H. The length of an array is stored in memory location 5000H. Store the largest number in memory location 400AH. [4]
  
2.
  - a. Write down the basic steps for interfacing an input device? [2]
  - b. Explain memory mapped I/O and peripheral mapped I/O technique with example. [2]
  - c. Design an interfacing I/O device using memory mapped I/O technique. The circuit should include one input port with 8 DIP switches and one output port to control 8 different appliances (assume the appliances). The appliances are turned on and off according to the corresponding switch positions. For example, the switch  $S_7$  connected in input port 7 should control the appliances connected in output port at position 7. All input switches are tied high, hence when the switch is OFF it has +5V and it has logic 0 when the switch is ON. Draw a detailed interfacing circuit, mention port addresses and write complete instructions. [6]
  
3.
  - a. Explain operation of interfacing an 8-bit A/D converter ADC0801 using an interrupt and draw a timing diagram to read data from A/D converter. [4]
  - b. Write a program and show calculations to calculate the delay of 2ms. [2]
  - c. Explain the content of RET instruction located at 2065H and show the bus and register contents. [4]
  
4.
  - a. Draw and explain the detailed internal block diagram of 8086. Define pipelining and how does it help in increasing the speed of execution. [4]
  - b. Write ALP in 8086 to transfer a block of data from one location to another [3]
  - c. Explain synchronous and asynchronous mode of transmission. Why do we use line drivers in transmission using RS-232 standard? [3]

P.T.O.

5.

- a. Design an interfacing circuit to read data from ADC0801 A/D converter using 8155A and display data in seven segment LED to meet following requirements. [6]
- Set PORT A as an input port in handshake mode to read data from A/D converter.
  - Set PORT B as an output port to display data at seven segment LEDs.
  - Use line PC<sub>5</sub> from PORT C to initiate conversion.
  - Use 8155 timer to record conversion time.
- b. Draw the expanded block diagram of 8155. Explain the operation of different modes of timer in 8155. [4]