Marks scored:

KATHMANDU UNIVERSITY
End Semester Examination [C]
July, 2017

Level : B. E.
Year : III
Course : EEEG 314
Semester : I
Exam Roll No. :
Time: 30 mins.
F. M. : 20
Registration No.:
Date JUL 14 2017

SECTION "A"
[20 Q. × 1 = 20 marks]

Encircle the most suitable answer to the following questions:

1. The number of interrupt lines in 8085 is _____
   a) 1 b) 2 c) 3 d) 5

2. The operating modes of 8255A are called _____.
   a) mode 0 and mode 1
   b) mode 0, mode 1 and mode 2
   c) mode 0 and mode 2
   d) mode 0, mode 2 and mode 3

3. Basic steps of execution of an instruction is _____.
   a) Fetch → execute → decode
   b) decode → fetch → execute
   c) execute → fetch → decode
   d) fetch → decode → execute

4. The CPU sends out a _____ signal to indicate that valid data is available on data bus.
   a) read b) write c) ALE d) INTR

5. When RET instruction is executed by a subroutine then _____.
   a) The top of the stack will be popped out and assigned to the PC.
   b) Without any operation, the calling program would resume from instructionimmediately following the call instruction.
   c) The PC will be incremented after the execution of the instruction.
   d) Without any operation, the calling program would resume from instructionimmediately following the call instruction and also the PC will be incrementedafter the execution of the instruction.

6. _____ Segment registers need to be initialized in an 8086/88 assembly program.
   a) CS and DS b) DS and ES c) DS and SS d) CS and SS

7. _____ Instruction is not possible in 8085.
   a) POP PSW b) POP B c) POP D d) POP 30H

8. _____ T-states are required for execution of OUT 80H instruction?
   a) 13 b) 10 c) 7 d) 12

9. Data storage in stack is designed in _____ method.
   a) FIFO b) LILO c) FILO d) LIFO

10. _____ machine cycles are required for execution of IN 30H instruction
a) 3 b) 4 c) 5 d) 6

11. _____ Instruction is required to rotate the content of accumulator one bit right along with carry.
a) RLC b) RAR c) RRC d) RAL

12. Temporary registers in 8085 are _____.
a) B and C b) D and E c) H and L d) W and Z.

13. There are _____ numbers of output pins in 8085 microprocessor.
a) 13 b) 27 c) 30 d) 40

14. RST 3 interrupts transfers program execution to _____ memory location.
a) 0000H b) 0008H c) 0018H d) 0038H

15. The execution of RST instruction causes the stack pointer to _____.
a) Increment by 2 b) decrement by 2 c) remain unaffected d) increment by 1

16. _____ Ports of PORTC are used to operate PORT A in handshake mode in 8155.
a) PC3 - PC5 b) PC0 – PC2 c) PC0 – PC6 d) PC2 - PC5

17. 8086 processor has _____ address pins out of which _____ numbers of pins are used as data pins.
a) 16, 8 b) 16, 14 c) 20, 16 d) 20, 8

18. During OPCODE fetch the state of S0 and S1 is _____.
a) 00 b) 10 c) 10 d) 11

19. The microprocessor issues ALE during first T-state of _____.
a) Fetch cycle only b) memory read cycle only
c) memory write cycle only d) every machine cycle

20. _____Interrupt is only edge sensitive.
a) RST 7.5 b) TRAP c) RST 6.5 d) RST 5.5