KATHMANDU UNIVERSITY
End Semester Examination
August/September 2017

Mark Scored :

AUG 31 2017

Level : B. E.
Year : II

Course : EEEG 214
Semester : II

Exam. Roll No. :

Time: 30 mins.

F. M. : 20

Registration No.:

Date :

SECTION "A"
[20 Q. × 1 = 20 marks]

Choose the best answer.

1. In an amplifier, series/shunt feedback _____ the input impedance and _____ the output impedance.
   [a] decreases, decreases
   [b] decreases, increases
   [c] increases, decreases
   [d] increases, increases

2. Neglecting early effect, the structure shown in Figure 1 has _____ feedback.
   [a] series/series [b] series/shunt [c] shunt/shunt [d] no

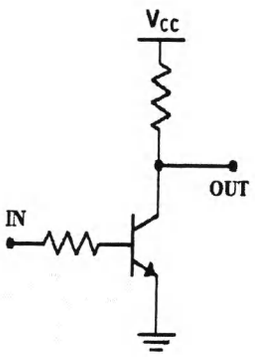


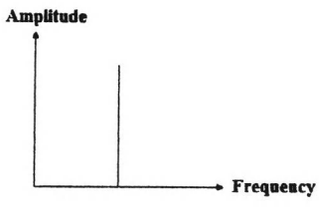
Figure: 1

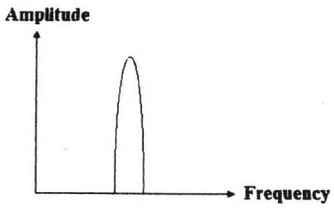
3. Negative feedback in an amplifier _____.
   [a] makes the system unstable
   [b] increases the system bandwidth
   [c] decreases the input impedance
   [d] increases the input impedance

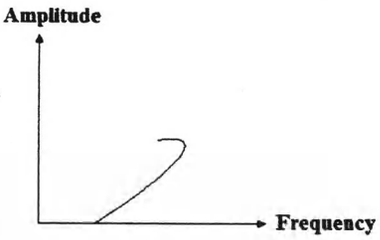
4. Negative feedback in an amplifier is effective only when _____, where G is the gain of an amplifier and H is the feedback fraction.
   [a] GH << 1 [b] GH = 0 [c] GH = 1 [d] GH >> 1

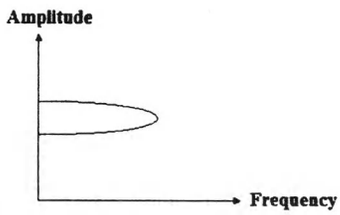
5. In an oscillator, the loop oscillates at the frequency in which the phase is _____.
   [a] 90^o [b] 180^o [c] 270^o [d] 360^o

6. Which of the following is an ideal oscillator response?

[a] 

[b] 

[c] 

[d] 

7. Schmitt trigger can convert _____.
[a] low frequency sine wave to high frequency sine wave
[b] sine wave to square wave
[c] square wave to sine wave
[d] sine wave to triangle wave

8. Harmonic oscillators basically generate _____signal.
[a] sine [b] square [c] triangular [d] delta

9. In a crystal oscillator, normally parallel resonating frequency is _____ series resonating frequency.
[a] lower than [b] higher than [c] equal to [d] an inverse of

10. The maximum voltage at the output of operational amplifier based logarithmic amplifier is _____ volts.
[a] 0.2 [b] 0.4 [c] 0.6 [d] 0.8

11. _____ is an ideal multiplier.
[a] $Z = XY+X^2$ [b] $Z = XY+Y^2$ [c] $Z = kXY$ [d] $Z = 2 + XY$

12. In general, in a PLL, capture range is _____ lock range.
[a] equal to [b] greater than
[c] smaller than [d] greater than or equal to

13. To control output frequency by input voltage, _____ is used.
[a] amplifier [b] phase detector [c] PLL [d] VCO

14. _____ is commonly used as frequency synthesizer.
[a] Filter [b] PLL [c] Amplifier [d] Precision rectifier

15. The delay power product of a logic gate is always _____.
[a] constant [b] infinity
[c] bias current dependent [d] unity

16. Precision rectifiers are used to _____.
[a] filter signal [b] rectify signal
[c] amplify and rectify signal [d] attenuate and rectify signal

17. In a Voltage Transfer Characteristics (VTC) of a CMOS inverter there are _____regions of operation.
[a] three [b] four [c] five [d] six

18. In a basic two-input CMOS NAND gate, there are _____ PMOS and _____ NMOS transistors.
[a] 2, 1 [b] 3, 3 [c] 2, 2 [d] 1, 2

19. The static power dissipation in a CMOS inverter is _____watts.
[a] 0 [b] $10I_DV_{DD}$ [c] 2 [d] 0.6

20. The basic fabrication material of a semiconductor IC is _____.
[a] sand [b] clay [c] iron [d] carbon

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SECTION "B"
[5 Q. × 11 = 55 marks]

Attempt *ANY FIVE* questions. Symbols have their usual meaning. Assume suitable data if necessary.

1. a. With reference to the block diagram of Figure 1, show that the stability of the amplifier increases with the application of negative feedback. [5]

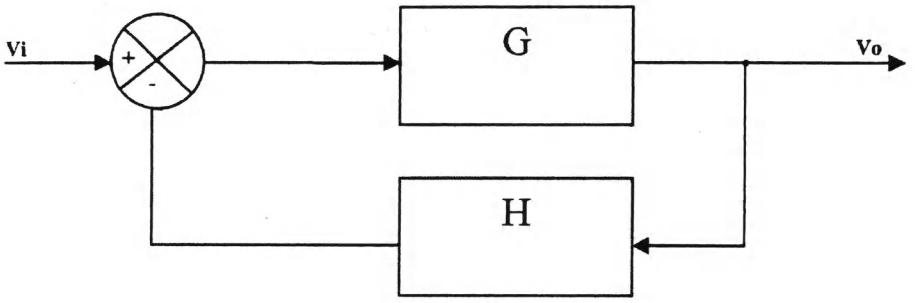

Figure: 1

b. For the circuit of Figure 2, find the approximate voltage gain. [6]

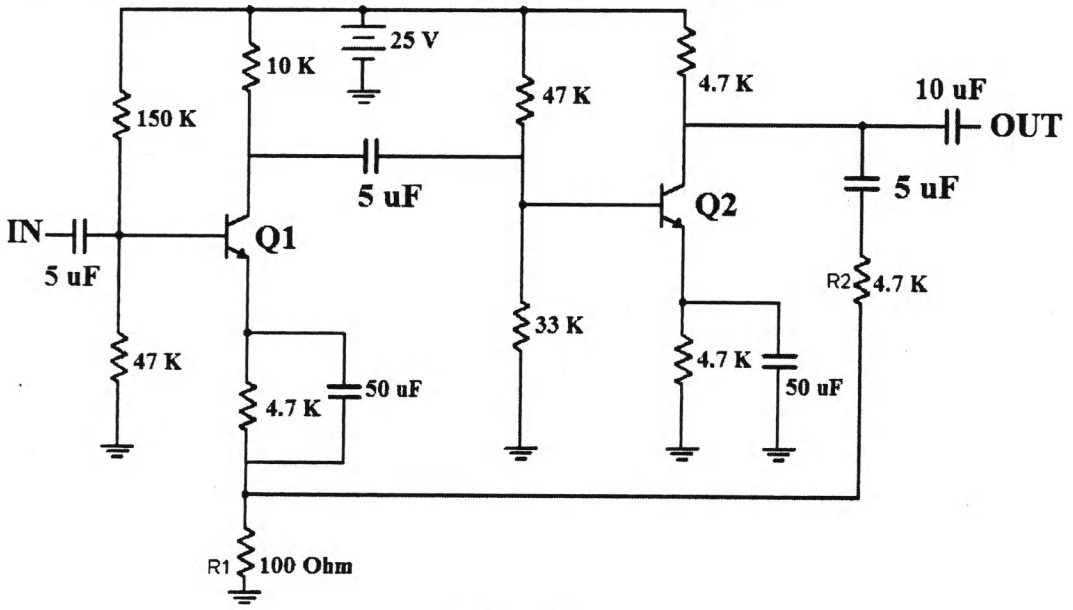

Figure: 2

2. a. Find the condition of oscillation for [5]

$$A = -Rf / Ri \text{ and}$$

$$\beta = R^3C^3S^3 / (R^3C^3S^3 + 6R^2C^2S^2 + 5RCS + 1)$$

b. Derive the frequency of oscillation for a Colpitts oscillator. [6]

3. a. Explain the working of circuit in Figure 3 and draw the exact waveforms at point A and point B. [5]

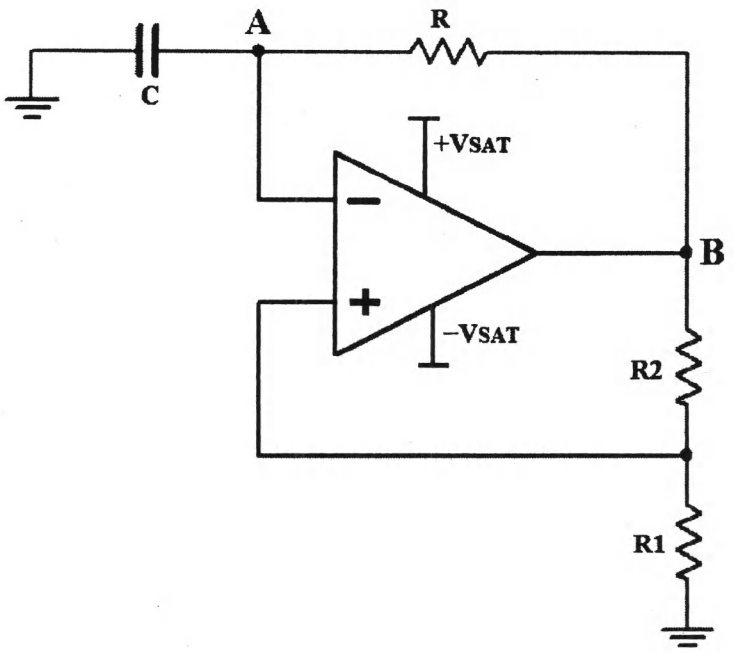

Figure: 3

b. Use the mathematical expression log (x) + log (y) = log (xy) to develop a circuit of multiplier. [6]

4. a. Design, with explanation, the operation of DTL based NAND gate. [5]
b. Design a circuit of CMOS NOT gate and draw its Voltage Transfer Characteristics. [6]

5. a. With circuit show that the power delay product of a logic circuit is always constant. [5]
b. Write all the fabrication steps of npn bipolar junction transistor. [6]

6. a. Design and explain a circuit to half wave rectify a sinusoidal waveform with 1mV peak. [5]
b. Design a Schmitt trigger using operational amplifier and also draw its Voltage Transfer Characteristics. [6]