SoE.
25 MAR 2025

KATHMANDU UNIVERSITY
End Semester Examination
March, 2024

Marks Scored:

Level : B.E.
Year : II

Course : EEEG 211
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date :

SECTION "A"
[20Q. × 0.5 = 10 marks]

Choose the most appropriate answer. Symbols have their usual meanings.

1. In a PN junction diode, if both the P and N regions are heavily doped, the depletion layer becomes:
   a. Wider
   b. Narrower
   c. Unchanged
   d. Dependent on junction area

2. The forbidden gap between valence and conduction band for GaAs is____.
   a. 0.67 eV
   b. 1.1 eV
   c. 1.2 eV
   d. 1.43 eV

3. In a half-wave rectifier circuit, the average (DC) output voltage is approximately:
   a. Vmax/π
   b. Vmax/2
   c. 0.45*Vmax
   d. 0.71*Vmax

4. The theoretical rectification efficiency of a half-wave rectifier is about:
   a. 30%
   b. 40%
   c. 70%
   d. 80%

5. In a full-wave bridge rectifier supplied by a 60 Hz AC source, the output ripple frequency is:
   a. 30 Hz
   b. 60 Hz
   c. 120 Hz
   d. 240 Hz

6. In a common emitter amplifier, the midband voltage gain (ignoring phase) is approximately given by:
   a. the ratio of the emitter resistor to the collector resistor
   b. the ratio of the collector resistor to the emitter resistor
   c. the transistor's current gain (β)
   d. the product of the transconductance (g_m) and the collector resistor

7. Which transistor biasing configuration is most effective in providing thermal stability?
   a. Fixed bias
   b. Emitter bias
   c. Voltage-divider bias
   d. collector to base bias

8. The primary function of a coupling capacitor in transistor amplifiers is to:
   a. Block DC while passing AC signals
   b. Filter out high-frequency noise
   c. Stabilize the biasing point
   d. Increase the overall power gain

9. The DC load line in BJT amplifier design is used to determine:
   a. The maximum power dissipation of the transistor
   b. The operating (Q) point of the transistor
   c. The frequency response of the amplifier
   d. The input impedance of the circuit

10. Which transistor biasing method is least sensitive to variations in the transistor's current gain (β)?
   a. Fixed bias
   b. Collector-feedback bias
   c. Voltage-divider bias
   d. Emitter bias

11. The maximum theoretical efficiency of a single-ended Class A power amplifier is approximately:
   a. 25%
   b. 33%
   c. 50%
   d. 100%

12. In a Class B power amplifier, each output device conducts for approximately:
   a. 180° of the input cycle
   b. 360° of the input cycle
   c. 90° of the input cycle
   d. 270° of the input cycle

13. The major disadvantage associated with Class B amplifiers compared to Class A is:
   a. Lower power efficiency
   b. Crossover distortion
   c. Higher idle power consumption
   d. Limited output power

14. In a BJT amplifier, bypassing the emitter resistor with a capacitor during AC operation will:
   a. Reduce the voltage gain
   b. Increase the voltage gain
   c. Leave the voltage gain unchanged
   d. Cause phase inversion

15. The input offset voltage of an Op-amp is defined as:
   a. the voltage required to null the output when both inputs are grounded
   b. the output voltage when the inputs are shorted
   c. the voltage difference between the supply rails
   d. the differential input voltage needed to force the output to zero

16. In the context of an operational amplifier, the term "slew rate" refers to:
   a. the maximum rate at which the output voltage can be changed.
   b. the total voltage gain of the amplifier at high frequencies.
   c. the delay between the input and the output signal.
   d. the ratio of the output voltage to the input voltage at DC.

17. In a Junction FET (JFET), increasing the reverse bias voltage applied to the gate results in:
   a. an increase in the conduction channel width
   b. a significant rise in drain current
   c. a reduction of the channel conduction area leading toward pinch-off
   d. forward biasing of the gate–channel junction

18. In rectifier circuits, the reverse recovery time of a diode is important because it:
    a. determines the forward voltage drop
    b. limits the maximum reverse current
    c. controls the breakdown voltage
    d. affects the high-frequency performance and switching speed

19. In a full-wave rectifier using a center-tapped transformer, conduction occurs in:
    a. one half of the secondary winding at a time
    b. both halves of the secondary winding simultaneously
    c. alternating cycles on the same half-winding
    d. only during the positive half-cycle of the input

20. For an n-channel enhancement-mode MOSFET to conduct, which of the following conditions must be satisfied?
    a. the drain–source voltage (V_{DS}) must be zero
    b. the gate–source voltage (V_{GS}) must be negative
    c. the gate–source voltage (V_{GS}) must be less than the threshold voltage (V_{TH})
    d. the gate–source voltage (V_{GS}) must exceed the threshold voltage (V_{TH})