

KATHMANDU UNIVERSITY
End Semester Examination
June/July, 2023

Marks Scored:

Level : B.E./B.Sc.
Year : II

Course : EEG 211
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date : 30 JUN 2023

SECTION "A"

[20 Q. \times 0.5 = 10 marks]

Encircle the most appropriate answer. Symbols have their usual meanings.

1. A semiconductor is formed by _____ bonds.
a. electrovalent b. covalent c. ionic d. electronic
2. Addition of pentavalent impurity to a pure semiconductor creates many _____.
a. free electrons b. valence electrons c. free holes d. bound holes
3. During the construction of BJT, _____ is made the smallest in size.
a. collector b. emitter c. base d. gate
4. For a JFET, when V_{DS} is increased beyond the pinch off voltage, the drain current _____.
a. remains constant b. decreases
c. increases d. first decreases and then increases
5. Rectification efficiency of a full-wave rectifier without filter is nearly equal to _____.
a. 41 % b. 61 % c. 71 % d. 81 %
6. Which of the following parameters will be very high in the common base configuration of a bipolar junction transistor?
a. current gain b. voltage gain c. input resistance d. output resistance
7. The input impedance of a transistor is _____.
a. very high b. high c. almost zero d. low
8. The current amplification factor in CE configuration is _____.
a. α b. $\beta+1$ c. β d. γ
9. In BJT, the equation $I_C = \alpha I_E +$ _____.
a. I_B b. I_{CBO} c. I_{CEO} d. βI_B
10. Bipolar Junction Transistors (BJTs) are _____.
a. gated controlled devices b. voltage controlling devices
c. both (a) and (b) are correct d. current controlling devices

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Level : B.E./B.Sc.
Year : II
Time : 2 hrs. 30 mins.

Course : EEEG 211
Semester : I
F. M. : 40

SECTION "B"
[5Q × 8 = 40 marks]

Attempt *ANY FIVE* questions. Symbols have their usual meanings. Assume suitable data if necessary.

1.
 - a. Discuss the operation of 6-0-6 full-wave rectifier circuit and calculate its efficiency.
 - b. Explain the operation of positive clamper circuit with waveform.

2.
 - a. Determine R_C , R_E , R_B , & V_{CEQ} for Figure 1.
 - b. Draw one common emitter type single stage voltage divider amplifier and derive the expression for the following parameters:
 - i. Input impedance (Z_i)
 - ii. Output impedance (Z_o)
 - iii. Voltage Gain (A_v)

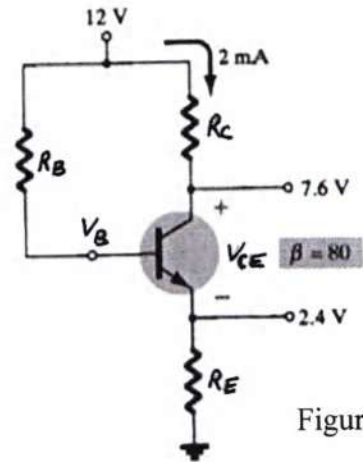


Figure 1

3.
 - a. Explain the construction and working principle of D-MOSFET with its drain characteristics.
 - b. Determine the required values of R_D and R_S for a given circuit in Figure 2 to maintain the drain current of 2.5 mA.

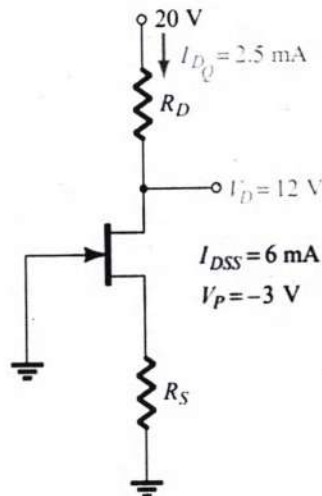


Figure 2

4.

- a. Using the information provided in Figure 3, Determine I_C , V_E , V_B and R_1

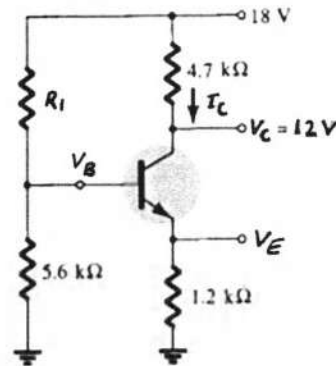


Figure 3

- b. Design an amplifier circuit having gain of 10, using BJT transistor.
- 5.
- a. Draw and explain the circuit diagram of transformer coupled class-A NPN power amplifier. Discuss about the cross-over distortion problem.
- b. Derive the expression for efficiency of transformer-coupled class B amplifier. For a class B amplifier using a supply of $V_{CC} = 30V$ and driving a load of 8Ω , determine the maximum input power, output power and efficiency.
- 6.
- a. Discuss any four ideal characteristics of Op-Amp. Derive the expression for integrating operational amplifier.
- b. Design an n-number of input summer operational amplifier-based circuit to obtain $V_O = 20(V_1 + V_2 + V_3 + V_2 + \dots + V_n)$, where, V_O is the output, V_1 , V_2 and V_3 are three inputs.