KATHMANDU UNIVERSITY
End Semester Examination [C]
November, 2018

Marks scored:

Level : B.E./ B.Sc.
Year : II

Course : EEEG 202
Semester: I

Exam Roll No. :

Time: 30 mins

F.M. : 20

Registration No.:

Date : NOV 15 2018

SECTION "A"
[20×1=20 marks]

Choose the most appropriate option. Symbols have their usual meaning.

1. If three input NOR gate has eight input possibilities, how many of those possibilities will result high output?
   a. 1 b. 2 c. 3 d. 7

2. The binary equivalent of decimal number 41.6875 is_____
   a. 101000.1011 b. 101001.1010 c. 101011.101 d. 101001.1011

3. If A and B are not inputs to the two input X-NOR gate, which of the following expression for output is correct?
   a. $\bar{A}B + A\bar{B}$ b. $\bar{A}\bar{B} + A\bar{B}$ c. $\bar{A}B - A\bar{B}$ d. $\bar{A}\bar{B} + AB$

4. Which of the following Boolean postulate is true?
   a. $X + 1 = X$ b. $X + 1 = 1$ c. $X + 1 = 1$ d. $X + 1 = 0$

5. TTL operates from a _____
   a. 12 - Volt supply b. 9 - Volt supply c. 5 - Volt supply d. 3 - Volt supply

6. 2's complement of decimal number 1101100 is given by
   a. 1010100 b. 0010100 c. 0010101 d. 0010000

7. Which of the following expression represents the Simplified Boolean function for the function $F(A,B,C) = \sum(1,2,3,5,7)$
   a. $F = A + \bar{A}B$ b. $F = A + AB$ c. $F = A + \bar{C}B$ d. $F = B + \bar{A}B$

8. Which of the following is universal logic gate?
   a. AND b. OR c. AND d. NAND

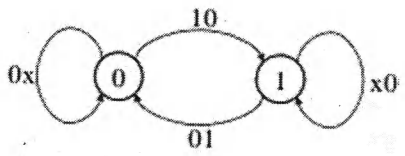
9. Which of the following binary combination represents the result of BCD addition of two BCD numbers 0100 and 1000?
   a. 10010 b. 0 1100 c. 10001 d. 10111

10. A ROM internally includes programmable OR gates and _____
    a. AND gates b. X-OR gates c. An encoder d. A Decoder

11. Flip flop conversion expressions for D flip flop to T flip flop is given by
    a. $D = T\bar{Q} + \bar{T}Q$ b. $D = T\bar{Q} + Q$ c. $D = T\bar{Q} + \bar{T}$ d. $D = T\bar{Q} + \bar{T}\bar{Q}$

12. The characteristic equation for the T flip flop is given by
    a. $Q(t+1) = J\bar{Q} + KQ$ b. $Q(t+1) = J\bar{Q} + \bar{K}Q$
    c. $Q(t+1) = \bar{J}\bar{Q} + \bar{K}\bar{Q}$ d. $Q(t+1) = \bar{J}\bar{Q} + \bar{K}Q$

13. The following figure represents the state transition diagram of _____



a. SR flip-flop b. D flip-flop c. T flip-flop d. JK flip-flop

14. For JK flip flop with J=1, K=1, the output after clock pulse will be_____
a. Low b. High c. No change d. Complimented

15. An encoder has maximum _____ input lines for N output lines.
a. N b. N^2 c. 2^N d. N-1

16. A 3 bit synchronous up counter counts up to _____
a. 3 b. 6 c. 7 d. 8

17. Mod-6 asynchronous up counter requires_____ flip flops.
a. 6 b. 5 c. 4 d. 3

18. Which of the following expression is correct for the given K-Map?

AB\CD	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	1	1	0	0
10	1	1	0	0

a. $F = \overline{A}$ b. $F = \overline{B}$ c. $F = \overline{C}$ d. $F = \overline{D}$

19. BCD input 0110 is fed to a seven segment display through BCD to seven segment decoder/driver. The segments which will lit up are:
a. a,b,d,e,f b. a,b,c,d,e,f c. all d. a,c,d,e,f,g

20. A 5 bit serial input serial output shift register requires .....
a. 4 SR flip flops b. 5 JK flip c. 5 D flip flops d. 4 D flip flops

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SECTION "B"
[5 Q.×11=55 marks]

Attempt any FIVE questions.
Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable.

1.
a. Differentiate between half adder and full adder and design logic circuit for full adder. [6]
b. Using 10's complement, subtract (a) 3250 – 72532 (b) 72532-3250 [3]
c. Verify the Boolean expression, $x + yz = (x+y)(x+z)$ [2]

2.
a. Simplify the following Boolean function using K-map
$F(w,x,y,z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$ and implement the resulting expression with NOR gates. [6]
b. Draw truth table and design 4 to 1 line multiplexer circuit. [5]

3.
a. Construct 4X16 decoder with two 3X8 decoder. [3]
b. Design logic circuit for 3 bit gray code to binary converter. [3]
c. Describe the working of serial in serial out shift register with circuit diagram and timing diagram. [5]

4.
a. Design a logic circuit that has four inputs W, X, Y, Z and an output that is to be high only when input Z is low and at the same time other any two inputs are high. [6]
b. Draw the state transition diagram of SR flip-flop and D flip-flop. [2]
c. Implement the following Boolean functions using ROM
$F_1(A,B,C) = \sum(0,1,2,4)$ and $F_2(A,B,C) = \sum(0,5,6,7)$ [3]

5.
a. Design a logic circuit for mod-8 synchronous up counter and explain the operation using timing diagram. [5]
b. Draw the characteristic table and excitation table for JK flip-flop. With the help of conversion expression, construct T flip-flop from the D flip-flop. [6]

6.
a. Design a logic circuit for mod-6 asynchronous up/down counter and explain the operation. [5]
b. A sequential circuit has two D flip-flops A and B, one input X and output Y. The circuit is described by the following flip-flop input output equations:
$D_A = AX+BX$, $D_B = AX + B'X$ and $Y = AB$. Draw the state table and state diagram of the circuit. [6]