KATHMANDU UNIVERSITY
End Semester Examination [C]
May/June, 2019

30 MAY 2019

Level : B.E./B.Sc.
Year : II
Time : 2 hrs. 30 mins.

Course : EEEG 202
Semester : I
F.M. : 55

SECTION "B"
[5Q × 11 = 55 marks]

Attempt *ANY FIVE* questions.
Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable. **Calculators are not allowed.**

1.
a. What is a reflected code? Find the (r-1)'s complement of $(25.639)_{10}$. [4]
b. Represent the decimal number 8620 (a) in BCD, (b) in excess-3 code and (c) in 2, 4, 2, 1 code. [3]
c. Explain duality principle. Prove that De-Morgan's theorem holds true for more than two variables. [4]

2.
a. Express the Boolean function $F = xy + x'z$ in a product of max term form. [3]
b. Show that the dual of the exclusive-OR is equal to its complement. [3]
c. Simplify the Boolean function F using the don't care conditions d, in (1) sum of products and (2) product of sums. [5]

$$F = A'B'D' + A'CD + A'BC$$
$$d = A'BC'D + ACD + AB'D'$$

3.
a. Point out the steps involved in a design procedure of a combination circuit. [3]
b. Design a combinational circuit to check for even parity of four bits. [4]
c. Obtain the NAND logic diagram of a full-adder from the Boolean function. [4]

$$C = xy + xz + yz$$
$$S = C'(x + y + z) + xyz$$

4.
a. Explain the special characteristics of IC digital logic families. [3]
b. Derive an equation for output carry for a full-adder circuit using look-ahead carry principle. [4]
c. Design a BCD-to-decimal decoder to give an output of all 0's when any invalid input combinations occur. [4]

5.
a. Explain register and its types with figure. [3]
b. Design a sequential circuit described by the following state equations. Use JK flip-flops. [5]

$$A(t+1) = xAB + yA'C + xy$$
$$B(t+1) = xAC + y'BC'$$
$$C(t+1) = x'B + yAB'$$

c. A combinational circuit is defined by the following three functions: [3]

$$F_1 = x'y' + xyz'$$

$$F_2 = x' + y$$

$$F_3 = xy + x'y'$$

Design a combination circuit using a ROM.

6.

a. Consider a register A and register B. How is it possible to move the contents of A into B using a serial operation? Explain with proper example and timing diagram. [4]

b. How can we use decoder as a demultiplexer? [2]

c. Construct a mod-8 asynchronous up counter. [5]

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Exam Roll No. :
Time: 30 mins.
F. M. : 20

Registration No.:
Date 30 MAY 2019

SECTION "A"
[20 Q × 1 = 20 marks]

Encircle the most suitable answer to the following questions. ***Calculators are not allowed.***

1. To use three input NAND gate as an inverter, _____.
   [a] any two inputs are kept open
   [b] any two inputs are connected to ground
   [c] any two inputs are connected to logic
   [d] any two inputs are connected to input

2. A bulb in a staircase has two switches, one switch is at ground floor and another is at first floor. The bulb can be turned on and also can be turned off by any one of the switches. This logic resembles_____.
   [a] an OR gate [b] an AND gate [c] an XOR gate [d] an X-NOR gate

3. The NAND - NAND realization is equivalent to _____.
   [a] AND - OR realization [b] AND - NOT realization
   [c] OR - AND realization [d] NOR - OR realization

4. If $(11X1Y)_8 = (12C9)_{16}$, the values of X and Y are _____.
   [a] 5 and 1 [b] 1 and 5 [c] 7 and 5 [d] 5 and 7

5. Excess 3 code is _____.
   i. BCD code ii. self-complementing code iii. unweighted code
   [a] i only [b] i and iii [c] iii only [d] i, ii and iii

6. In NOR-NOR configuration, the minimum number of NOR gates needed to implement F = A+ AB'+AB'C is _____
   [a] 2 [b] 5 [c] 3 [d] 0

7. The expression A = X'Y'Z' is equivalent to which single gate?
   [a] NAND [b] NOR [c] OR [d] AND

8. If an eight bit ring counter has initial state of 10111110, _____ is the state after fifth clock pulse.
   [a] 11101011 [b] 11110101 [c] 10101111 [d] 00010111

9. $(200)_{12} - (100)_{11}$ is equal to _____.
   [a] $(167)_{10}$ [b] $(50)_{10}$ [c] $(100)_{10}$ [d] $(140)_{10}$

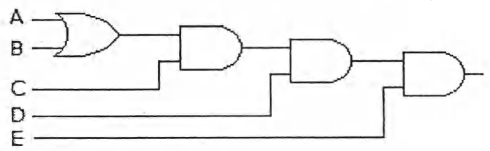
10. How many 3×8 decoders are required for a 1 of 32 decoder?
    [a] 1 [b] 2 [c] 4 [d] 8

11. To construct $2^n \times 1$ multiplexer, _____ number of 2×1 multiplexer are needed.
[a] n [b] 2^{2n} [c] 2^{n-1} [d] 2^n-1

12. A master-slave has the characteristic that _____.
[a] master is level triggered and slave is edge triggered
[b] master is edge triggered and slave is level triggered
[c] master is positive edge triggered and slave is negative edge triggered
[d] master is negative level triggered and slave is positive level triggered

13. The output frequency of a mod 16 counter clocked from a 20 KHz input signal is ___ .
[a]20 KHz [b] 120 KHz [c] 1250 Hz [d] 1.25 Hz

14. The expression given by the following circuit is _____.



[a] CDE(A+B) [b] ABCDE [c] [C(A+B)D]+E [d] C[(A+B)E]+D

15. D flip flop can be made from a JK flip flop by making _____.
[a] J = K [b] J = K =1 [c] J = 0,K =1 [d] J = K'

16. When does the race around condition arrive?
[a] clock pulse duration>propagation delay
[b] clock pulse duration<propagation delay
[c] clock pulse duration = propagation delay
[d] clock pulse duration<=propagation delay

17. Recording a music in a recorder is an example of _____.
[a] encoder [b] decoder [c] data storage [d] multiplexer

18. To create time delay, we use _____.
[a] synchronous circuits [b] clocked circuits
[c] non clocked circuits [d] asynchronous circuits

19. A 512×8 ROM has _____.
[a] 512 inputs and 8 outputs [b] 512 inputs and 3 outputs
[c] 9 inputs and 8 outputs [d] 9 inputs and 3 outputs

20. The main difference between a register and a counter is_____.
[a] A register has a specific sequence of states
[b] A register has no specific sequence of states
[c] A register has capability to store one bit of information but counter has n-bit
[d] A register shifts the data bit whereas counter does not.

KATHMANDU UNIVERSITY

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May 22, 2019

NOTICE

End-Semester Compartmental Examinations of B.E.\B.Sc.\B.Pharm.\B.Tech.\B.Arch. students will be held according to the following schedule.

Date	Day	Courses
May 30, 2019	Thursday	MATH 101, MATH 111, MATH 105, EEEG 202, BIOT 302, COMP 342, PHAR 301, PHAR 303, CHEG 302, MEEG 315, GEOM 316, CIEG 304, EPEG 302, ENVE 309, COMP 421, CIEG 401, CIEG 402
May 31, 2019	Friday	ENGT 101, CHEM 207, EEEG 213, MEEG 213, MATH 201, MATH 205, PHAR 204, CIEG 204, ARCH 204, MEPP 412, MEPP 430, COMP 484, COMP 486, ENVS 415, MGTS 403, GEOM 402, PHAR 408
June 2, 2019	Sunday	PHYS 101, ARCH 101, MCSC 201, EEEG 207, PHYS 202, CIEG 203, GEOM 205, BIOT 204, COMP 315, MGTS 301, COMP 317, PHYS 302, COMP 302, BIOT 401, BIOT 410
June 3 2019	Monday	MATH 207, BIOT 203, ENVS 201, PHAR 203, PHAR 404, COMP 472, COMP 478, ENVS 404, EPEG 413, CIEG 405, PHAR 401
June 4, 2019	Tuesday	COMP 103, COMP 101, PHYS 201, STAT 201, PHYS 203, MATH 322, COEG 304, INAN 301, CHEG 303, EPEG 422, BIOT 403
June 5, 2019	Wednesday	EEEG 204, CIEG 201, BIOT 202, ENVS 212, MEEG 217, COMP 307, COMP 314, CIEG 303, ETEG 402, MGTS 402, PHAR 406
June 6, 2019	Thursday	ENGG 111, BIOL 101, COMP 202, MATH 208, PHYS 206, PHAR 201, ENVS 207, GEOM 317, PHAR 304, MEEG 328, MEEG 301, COMP 401, COMP 407, GEOM 411, PHYS 404
June 7, 2019	Friday	EEEG 211, MEEG 216, BIOT 205, MATH 206, MATH 204, CIEG 202, MEEG 219, EEEG 313, CIEG 305, CIEG 406, ENVS 431, PHAR 402, PHYS 405
June 9, 2019	Sunday	CHEM 101, CHEM 201, ENVE 204, MEEG 218, EEEG 314, COEG 401

Examination Time : 11.00 A.M. to 2.00 P.M.
Center : Kathmandu University, Dhulikhel.

Prof. Panna Thapa, Ph. D.
Controller of Examinations