KATHMANDU UNIVERSITY
End Semester Examination
March, 2025

Level : B.Sc. 16-March-025 Course : EEEG 202
Year : II Semester : I
Time : 2 hrs. 30mins. F. M. : 40

SECTION "B"
[4Q. × 10 = 40 marks]

Attempt ANY FOUR questions. Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable.

1.
a. Simplify the following Boolean expression using the basic Boolean theorems: [3]
F (A, B, C) = (A+B) (A+B') (A'+C)
b. Using 10's complement, perform the following subtraction: [3]
$(470)_{10} - (231)_{10}$
c. Implement full adder using multiplexer. [4]

2.
a. Derive the characteristic equation of SR flip-flop and convert the SR flip-flop into JK flip-flop with the help of excitation table. [1+4]
b. Simplify the following Boolean function using K-map into (a) sum of products form and (b) product of sums form: [5]
$$F (A, B, C, D) = \sum(0,1,2,5,8,9,10)$$

3.
a. Explain the working of 4-bit parallel input serial output shift register with the help of circuit diagram. [5]
b. Draw the truth table and design a logic circuit for BCD adder. [5]

4.
a. Design a traffic light control system for two intersections with a special feature: **emergency vehicle override.** If an emergency vehicle is detected at any intersection, the corresponding intersection's green light should remain ON until the emergency vehicle passes (Make necessary assumptions if required). [4]

b. Differentiate between the synchronous and asynchronous counter. Draw the truth table and design a logic circuit for the 4 bit asynchronous up/down counter. Also, explain the operation of the designed counter using timing diagram. [6]

P.T.O.

5.

a. Express the following Boolean function F = xy + x'z as a product of maxterms. [4]

b. Draw the state table and state diagram of the following synchronous sequential logic circuit (Figure1): [6]

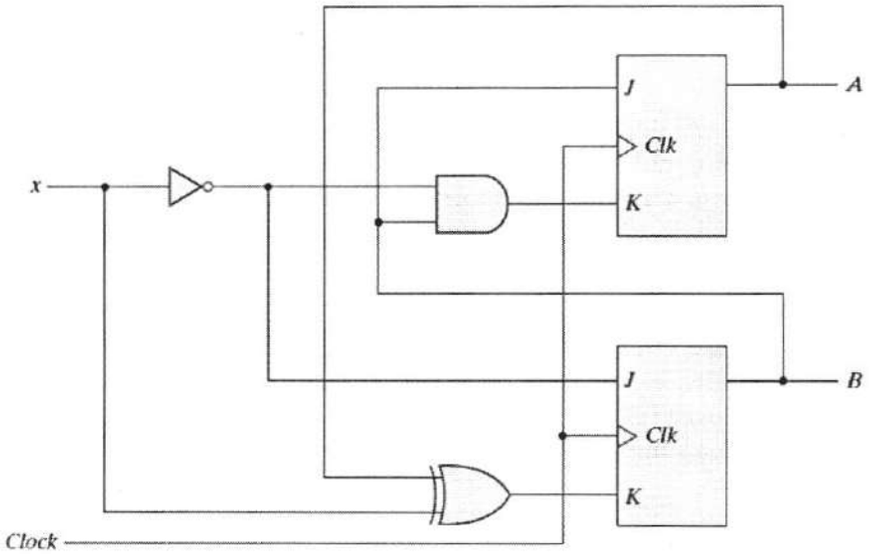

Figure1

KATHMANDU UNIVERSITY
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March, 2025

Marks Scored:

Level : B.Sc.
Year : II

Course : EEEG 202
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date : 16-March-025

SECTION "A"

[20 Q. × 0.5 = 10 marks]

Choose and **encirlce** in the most appropriate option. **Symbols** have their usual meaning.

1. For which of the following Boolean expression, the output is 1 when A= 0 and B = 1?
   a. AB + AB' b. AB' + A'B' c. AB + A'B' d. A'B + AB'

2. Which of the following is typically used in the internal structure of a ROM for addressing purposes?
   a. Flip-flops b. Multiplexer c. Encoder d. Decoder

3. The 10's complement of $(246700)_{10}$ is _____
   a. 999900 b. 753299 c. 753300 d. 864399

4. In a multiplexer, the output is determined by
   a. The number of input lines
   b. The number variables in Boolean Expression
   c. The number complemented variables in Boolean Expression
   d. The number of selection lines

5. How many Flip-Flops are required for mod–16 counter?
   a. 8 b. 6 c. 3 d. 4

6. The binary code for Gray code 1000 is equivalent to _____
   a. 0101 b. 1111 c. 1101 d. 1110

7. If x and y are Boolean variables then, x + xy equals to _____
   a. y b. x' c. y' d. x

8. The digital logic family which has minimum power dissipation is _____
   a. TTL b. RTL c. DTL d. CMOS

9. The number of outputs in a PLA is determined by
   a. The number of AND gates in the AND plane
   b. The number of OR gates in the OR plane
   c. The number of variables
   d. Complexity of Boolean expression

10. For 0100 and 1000, result of BCD addition is_____
    a. 1100 b. 10010 c. 10111 d. 10011

11. The simplified expression for F (A, B, C) =A'B+BC'+BC+AB'C' is _____
a. B+A'C' b. B'+AC' c. B+AC' d. B+AC

12. Which of the following decoders is used in BCD to decimal conversion?
a. 3-to-8 decoder b. 2-to-4 decoder c. 4-to-16 decoder d. 5-to-32 decoder

13. A N bit up counter counts up to _____
a. N b. 2^N c. N-1 d. 2^N -1

14. For SR flip flop with S=0, R=1, the output after clock pulse will be _____
a. Low b. High
c. No change d. Complement of previous state

15. What is the main purpose of a D flip-flop in digital circuits?
a. To count input pulses b. To generate clock pulses
c. To perform arithmetic operations d. To store one bit of data

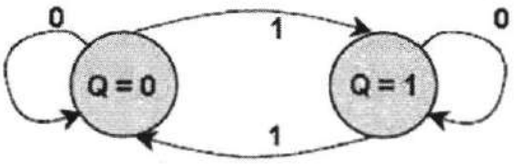
16. Which of the following expression is correct for the given K-Map?

AB\CD	00	01	11	10
00	1	1	1	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

a. $\overline{A}\,\overline{B}$ +BD b. AB+BD c. AB + $\overline{B}\,\overline{D}$ d. $\overline{A}\,\overline{B}$ +$\overline{B}\,\overline{D}$

17. Which of the following represents the characteristic equation of SR flip flop?
a. Q(next) = S + RQ b. Q(next) = S + R'Q
c. Q(next) = SR + RQ d. R + S'Q

18. The figure below represents the state transition diagram of _____



a. SR flip-flop b. JK flip-flop c. T flip-flop d. D flip-flop

19. How does a synchronous counter change its state?
a. At different clock edges for each flip-flop
b. Based on the same clock signal for all flip-flops
c. Randomly
d. By an external event

20. The 4-bit universal shift register requires four ____ flip-flops and four _____ multiplexers respectively
a. T, 4:1 b. D, 3:1 c. D, 4:1 d. JK, 4:1