SOE.

KATHMANDU UNIVERSITY
End Semester Examination
March, 2024

Marks Scored:

Level : B.E.
Year : II
Course : EEEG 202
Semester : I
Exam Roll No. :
Time: 30 mins.
F. M. : 10
Registration No.:
Date 21 MAR 2025

SECTION "A"
[20Q. × 0.5 = 10 marks]

Choose the most appropriate answer. Symbols have their usual meanings.

1. Minimum number of 2:1 multiplexer required to design 16:1 multiplexer is _____
   a. 8 b. 4 c. 15 d. 10

2. Binary number 101110110 is equal to decimal number _____.
   a. 468 b. 412 c. 374 d. 326

3. One megabyte in base 2 (binary) is equivalent to _____.
   a. 10^3 bytes b. 10^4 bytes c. 2^{10} bytes d. 2^{20} bytes

4. _____ condition in JK flip flop shows no change to next state from the present state.
   a. J=K=0 b. J=1, K=0 c. J=K=1 d. J=0, K=1

5. What is the 2's complement of the binary number 1101?
   a. 0011 b. 1110 c. 1011 d. 0101

6. _____decimal code represents each decimal digit with its equivalent binary number?
   a. Excess-3 b. BCD c. Gray code d. ASCII

7. What is the hexadecimal equivalent of the binary number 101101?
   a. 2D b. 3A c. 2C d. 1B

8. _____ Boolean algebra theorem states that A + A' = 1?
   a. Idempotent Law b. Complement Law
   c. Associative Law d. Absorption Law

9. _____logic gate produces a high output only when both inputs are low.
   a. NAND b. NOR c. XOR d. AND

10. _____ IC family consumes the least power?
    a. TTL b. CMOS c. ECL d. DTL

11. How many cells are there in a 4-variable Karnaugh Map?
    a. 8 b. 12 c. 16 d. 20

12. What does a "don't care" condition in a K-map indicate?
    a. It must always be 1
    b. It must always be 0
    c. It can be used as either 1 or 0 for simplification
    d. It is an invalid condition

13. _____combinational circuit is used for code conversion.
    a. Adder b. Decoder c. Encoder d. Multiplexer

14. _____ of the following circuits can store one bit of data.
    a. Flip-Flop b. Counter c. Multiplexer d. Comparator

15. What is the minimum number of NAND gates required to implement an XOR gate?
    a. 2 b. 3 c. 4 d. 5

16. _____ of the following is a hazard in digital circuits.
    a. Power dissipation b. Delay
    c. Glitch d. Fan-out

17. In a Johnson counter with 5 flip-flops, what is the number of unique states?
    a. 5 b. 10 c. 15 d. 20

18. What is the primary drawback of asynchronous sequential circuits?
    a. Expensive to implement
    b. High power consumption
    c. Unpredictable behavior due to race conditions
    d. Requires a clock signal

19. What is the function of a ring counter with 4 flip-flops?
    a. Counts from 0 to 15 b. Shifts data left
    c. Cycles through 4 unique states d. Acts as a binary adder

20. A 4-bit shift register is initially loaded with 1011. After three right shifts, what is the content?
    a. 0001 b. 0010 c. 0101 d. 1001

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SECTION "B"
[4 Q. × 10 = 40 marks]

Attempt *ANY FOUR* questions. Figure in the margin indicates the full marks. Students are required to answer in their own words as far as practicable.

1.

a. Determine the even-parity bit generated when the message consists of the ten decimal digits in the 8,4, -2,-1 code. [3]
b. A 3-bit sensor (T2, T1, T0) measures temperature from 0°C (000) to 7°C (111). Two outputs are needed: i) Heater (H) activates for temperatures ≤ 2°C ii) Cooler (C) activates for temperatures ≥ 6°C [3]
   i. Create separate K-maps for H and C
   ii. Derive simplified expressions for both outputs
c. Design a 3-bit odd-parity generator and a checker circuit. [4]

2.

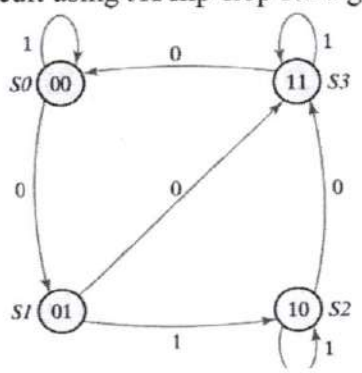
a. Implement a full subtractor with two half-subtractors and an OR gate. [3]
b. Design a combinational circuit that accepts a 3-bit number and generates an output binary equal to the square of the input number. [5]
c. Implement the Boolean function: $F = xyz' + xy' + yz$ using NAND gates. [2]

3.

a. Design a circuit of a 3-bit priority encoder. [3]
b. Implement a Full Adder using a PLA. [4]
c. Design a BCD-decimal decoder. [3]

4.

a. Design a sequential circuit using JK flip-flop for a given state diagram. [5]



b. Design a register with parallel load using D flip flops. [5]

P.T.O.

5.

a. Design a serial adder using sequential logic to add 4-bit binary number stored in shift register A and shift register B respectively. Store the sum in shift register A. [5]
b. Construct a Johnson counter with ten timing signals. [3]
c. Explain the working principle of a demultiplexer? [2]