KATHMANDU UNIVERSITY
End Semester Examination
March/April, 2017

Marks Scored:

Level : B. E.\ B.Sc.
Year : II
Course : EEEG 202
Semester : I
Exam Roll No. :
Time : 30 mins.
F. M. : 20
Registration No. :
Date : MAR 2 7 2017

SECTION "A"
[20 Q. × 1 = 20 marks]

Choose the most appropriate option. Symbols have their usual meaning.

1. The decimal equivalent of octal number 147.3 is
   a. 103.3 b. 201.4 c. 116.3 d. 234.4

2. How many bits are needed to represent an 8 digit hexadecimal number in BCD?
   a. 8 b. 16 c. 32 d. 64

3. If A and B are inputs to a two input X-NOR gate, which of the following expression for output is correct?
   a. $\bar{A}B + A\bar{B}$ b. $\bar{A}\bar{B} + A\bar{B}$ c. $\bar{A}B - A\bar{B}$ d. $\bar{A}\bar{B} + AB$

4. Which of the following Boolean postulate is true?
   a. X+YZ = (X+Y)(X+Z) b. X+YZ = XY+Z
   c. X+YZ = X(Y+Z) d. X+YZ = XYZ+YZ

5. The Gray code for decimal number 5 is equivalent to .....
   a. 0111 b. 0110 c. 0011 d. 0100

6. N bit register requires .....flip-flops.
   a. N b. 2N c. N+1 d. N^2

7. If a TTL output can only output logic low by sinking current, then this type of output is known as
   a. Totem-pole b. Try state c. Open collector d. Open emitter

8. Which of the following is universal gate?
   a. AND b. OR c. AND d. NOR

9. Which of the following binary combination represents the result of BCD addition of two BCD numbers 0100 and 1000?
   a. 1100 b. 10010 c. 1001 d. 10110

10. A 32x8 ROM internally includes .....OR gates.
    a. 2 b. 4 c. 6 d. 8

11. How many flip-flops are required for a mod-10 counter?
    a. 2 b. 3 c. 4 d. 5

12. A decoder with an enable input acts as
    a. a multiplexer b. a demultiplexer c. an encoder d. an adder

13. A device which converts BCD to Seven Segment is called
a. Encoder b. Decoder c. Multiplexer d. Demultiplexer

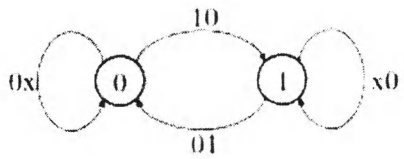
14. For JK flip flop with J=1, K=1, the output after clock pulse will be
a. Low b. High c. Unchanged d. Complimented

15. The excess-3 code of decimal 6 is represented by
a. 1001 b. 1011 c. 0101 d. 0110

16. When both inputs are same, invalid condition occurs in
a. SR flip-flop b. D flip-flop c. T flip-flop d. JK flip-flop

17. Flip-flops are memory device which store .....
a. One bit of information b. Two bits of information
c. Three bits of information d. More than two bits of information

18. The following figure represents the state transition diagram of



a. SR flip-flop b. D flip-flop c. T flip-flop d. JK flip-flop

19. Which of the following expression is correct for the given K-Map?

AB\CD	00	01	11	10
00	1	1	1	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

a. $\overline{B}\ \overline{A} + \overline{B}\ \overline{D}$ b. $\overline{B}\,C + \overline{B}\ D$ c. $B\ \overline{C} + B\ \overline{D}$ d. $\overline{B}\ \overline{C} + BD$

20. BCD input 1001 is fed to a seven segment display through BCD to seven segment decoder/driver. The segments which will lit up are:
a. a,b,d,e,f b. a,b,c,d,e,f c. all d. a,b,c,d,f,g

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Level : B. E.\ B.Sc. | Course : EEEG 202
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Time : 2 hrs. 30 mins. | F. M. : 55

SECTION "B"
[5 Q.× 11 = 55 marks]

Attempt *ANY FIVE* questions. Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable. Calculators are not allowed.

1.
a) Why are digital systems capable of greater accuracy than analog systems? [2]
b) How do you differentiate between binary logic and arithmetic logic? Implement output function of exclusive-OR gate with NAND gate. [1+2]
c) Design a logic circuit for BCD to excess-3 code converter. [6]

2.
a) State the duality principle and prove that
ab + bc + ac = (a+b) • (b+c) • (a+c) [1+4]
b) Design a half adder circuit using any one of the two universal gates. [4]
c) Convert $(16.425)_{10}$ into hexadecimal. [2]

3.
a) Simplify the following Boolean expression using tabulation method:
f (A,B,C) = A'B'C + A'BC' +A'BC +AB'C + ABC [3]
b) Write some applications of multiplexer and demultiplexer. Design a logic circuit for 4 to 1 line multiplexer. [1+4]
c) Design logic circuit for 3 bit binary to gray code converter. [3]

4.
a) Design a logic circuit that has three inputs and an output that is to be high only for input greater than 010 and less than 111. [4]
b) How is edge triggering achieved using master-slave flip-flop? [3]
c) Design a logic circuit for mod-6 synchronous up counter using T-flip-flop. [4]

5.
a) Differentiate between flip-flop and latch. Convert the SR flip-flop into the JK flip-flop with the help of excitation table. [2+4]
b) Design a logic circuit for mod-10 asynchronous down counter and explain the operation using timing diagram. [5]

6.
a) Classify the shift registers and explain the working of bidirectional shift register with circuit diagram. [5]
b) Differentiate between synchronous sequential circuit and asynchronous sequential circuit. A sequential circuit has two JK flip-flops, A and B, and one input, X. The circuit is described by the following flip-flop input equations:
$J_A = X$ $K_A = \overline{B}$ $J_B = X$ $K_B = A$
Draw the state table and state diagram of the circuit. [1+5]