KATHMANDU UNIVERSITY
End Semester Examination
July/August 2024

Level : B.E.
Year : II
Time : 2 hrs. 30mins.

29 JUL 2024

Course : EEEG 202
Semester : I
F. M. : 40

SECTION "B"
[4 Q. × 10 = 40 marks]

Attempt ANY FOUR questions. Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable. Calculators are not allowed.

1.
a. Design an asynchronous counter which counts from 0 to 10 and then from 12 to 15 (The counter is to skip the output 11). [5]
b. Using 10's complement, perform the following subtraction: (72532-3250) [2]
c. Express the following Boolean function, $F = xy + \bar{x}z$ as product of maxterms. [3]

2.
a. Simplify the following Boolean expression using K-Map and implement the resulting expression using only NOR gates: [4+2]
$F(A, B, C, D) = A\{\bar{C}(\bar{B}D + B\bar{D}) + BC\} + \bar{D}\{B(AC + \bar{A}\bar{C}) + \bar{A}\bar{B}\} + A\,\bar{C}\bar{D} + \bar{A}\,BD$
b. Write truth table and design logic circuit of even parity checker for three-bit generated message. [4]

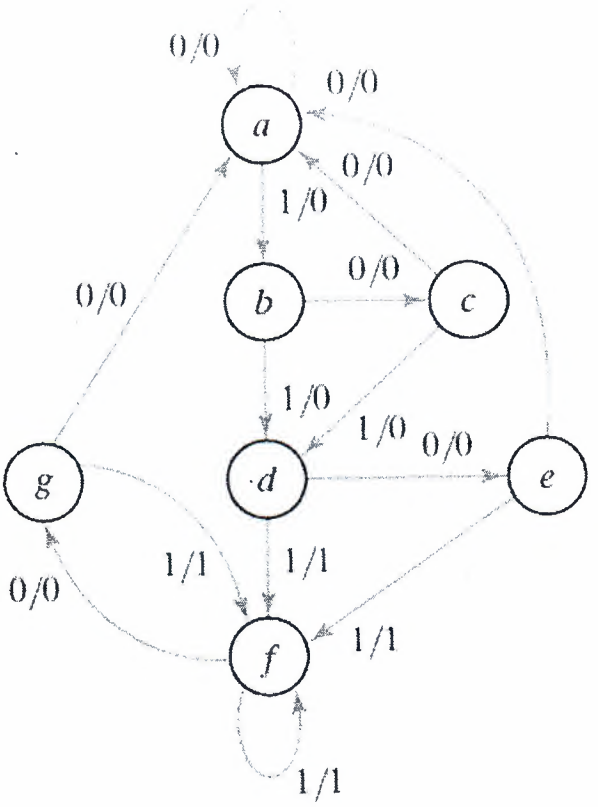
3.
a. Write the characteristic equation of JK flip-flop and convert the JK flip-flop to the D flip-flop with the help of conversion table. [1+4]
b. Design a logic circuit for mod-6 synchronous down counter and explain the working mechanism with the help of timing diagram. [5]

4.
a. Explain the working of 3-bit universal shift register with the help of circuit diagram. [5]
b. Design a combinational logic circuit for a BCD adder. [5]

5.
a. A combinational circuit has four inputs (A, B, C, D) and one output Z. The output is high when both first and second inputs (AB) are high or both third and fourth inputs (CD) are high. Draw a truth table and design a logic circuit using 8:1 multiplexer circuit. [4]

P.T.O.

b. Differentiate between the Mealy and Moore circuit and reduce the following state diagram: [6]



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Marks Scored:

Level : B.E.
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Exam Roll No. :
Time: 30 mins.
F. M. : 20

Registration No.:
Date 29 JUL 2024

SECTION "A"
[20Q. × 1 = 20 marks]

Choose and encircle the most appropriate option from each set of choices. Symbols have their usual meaning.

1. How many two input logic gates are required to construct the logic circuit for the following Boolean expression?
$F = ABC + \bar{A}B$
a. 6 b. 5 c. 4 d. 3

2. How many times will carry be generated and how many times will carry be propagated if 1111 is added to 1111, both being binary numbers?
a. 2,2 b. 3,4 c. 4,3 d. None of these

3. The 2's complement of $(0101)_2$ is _____
a. $(1010)_2$ b. $(1010)_2$ c. $(1011)_2$ d. $(1101)_2$

4. The number of control lines for an 8 to 1 multiplexer is _____
a. 2 b. 3 c. 4 d. 5

5. How many Flip-Flops are required for mod–12 counter?
a. 6 b. 5 c. 3 d. 4

6. The binary code for Gray code 0100 is equivalent to _____
a. 0101 b. 1010 c. 1101 d. 0111

7. If A is a Boolean variable then, A+1 equals to _____
a. A b 1 c. 0 d. 2A

8. The digital logic family which has minimum propagation delay is _____
a. TTL b. RTL c. DTL d. CMOS

9. If segments b, c, f and g are turned on for a seven segment display, the display will show _____
a. 7 b. 4 c. 3 d. 8

10. The BCD sum of two decimal numbers, 4 and 6 is _____
a. 1010 b. 10000 c. 10110 d. 10010

11. If A, B and C are the Boolean variables, which of the following expression is the simplified expression for the given Boolean expression, F (A, B, C)= $ABC + \bar{A} + A\bar{B}C$

a. $A + C$ b. $\bar{B} + D$ c. $\bar{A} + D$ d. $\bar{A} + C$

12. The device which changes from parallel data to serial data is _____

a. Encoder b. Decoder c. Multiplexer d. Demultiplexer

13. A mod-6 up counter counts up to _____

a. 5 b. 6 c. 25 d. 36

14. An asynchronous binary counter constructed with JK flip-flops counts from 0 to 255. How many JK flip-flops are necessary for this counter?

a. 255 b. 128 c. 32 d. 8

15. Flip-flops are memory device which store _____

a. One bit of information b. two bit of information

c. Three bit of information d. More than two bits of information

16. Which of the following expression is correct for the given K-Map?

AB\CD	00	01	11	10
00	1	1		0
01	0	X	0	0
11	0	0	0	0
10	1	1	0	0

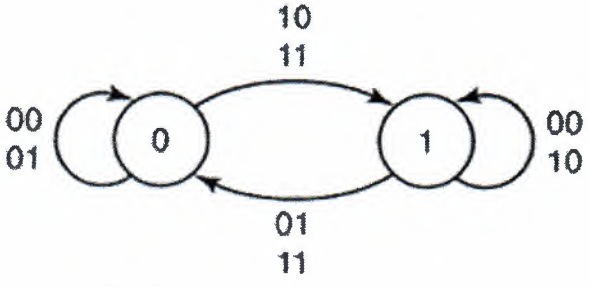
a. $\bar{A}\bar{B}$ b. $\bar{B}\bar{C}$ c. $\bar{B}\bar{C} + \bar{A}\bar{C}\bar{D}$ d. $\bar{B}\bar{C} + \bar{A}\bar{C}D$

17. Which of the following represents the characteristic equation of SR flip flop?

a. Q(next) = S + R'Q b. Q(next) = S + RQ

c. Q(next) = S' + R'Q d. Q(next) = S + RQ'

18. The figure below represents the state transition diagram of _____



a. SR flip-flop b. JK flip-flop c. T flip-flop d. D flip-flop

19. A decoder offers N inputs and maximum _____ output lines.

a. 2^{N-1} b. N^2 c. N d. 2^N

20. A 4-bit parallel input serial output shift register requires _____ D flip-flops and _____ OR gates respectively.

a. 4 and 6 b. 3 and 6 c. 4 and 3 d. 4 and 4