

KATHMANDU UNIVERSITY  
End Semester Examination  
June/July, 2023

Marks Scored:

Level : B.E./B.Sc.

Course : EEEG 202

Year : II

Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date : 26 JUN 2023

SECTION "A"

[20Q.  $\times$  0.5 = 10 marks]

Encircle the most appropriate option. **Symbols** have their usual meaning

- Which of these code pairs correctly represent Digital Electronics reflective codes?  
a. 2421 and 8421    b. 2421 and 5211    c. 5211 and 8421    d. 5421 and 2421
- The NOR gate output will be high if the two inputs are \_\_\_\_\_.  
a. 00    b. 01    c. 10    d. 11
- Which of the following is the simplified expression for  $AB+A(B+C)+B(B+C)$ ?  
a.  $A+AB$     b.  $B+AB$     c.  $A+AC$     d.  $B+AC$
- A blub in a staircase has two switches, one switch is at ground floor and another is at first floor. The blub can be turned on and also can be turned off by any one of the switches. This logic resembles the \_\_\_\_\_.  
a. OR gate    b. XOR gate    c. AND gate    d. X-NOR gate
- The number of selection lines required for a 1 – to – 16 demultiplexer is \_\_\_\_\_.  
a. 2    b. 3    c. 4    d. 5
- The digital logic family which has minimum power dissipation is \_\_\_\_\_.  
a. TTL    b. RTL    c. DTL    d. CMOS
- A priority encoder has four inputs  $I_0, I_1, I_2,$  and  $I_3$  where  $I_3$  has the highest priority and  $I_0$  has the least priority. If  $I_2 = 1$ , what will be the output?  
a. 00    b. 01    c. 10    d. 11
- For JK flip flop with  $J=0, K=1$ , the output after clock pulse will be \_\_\_\_\_.  
a. Low    b. High    c. No change    d. Invalid
- D flip flop can be made from a J-K flip flop by making \_\_\_\_\_.  
a.  $J=K$     b.  $J=K=1$     c.  $J=0, K=1$     d.  $J=K'$
- Flip-flops are memory devices which store \_\_\_\_\_.  
a. One bit of information    b. Two bit of information  
c. Three bit of information    d. More than two bits of information
- In a ripple counter, \_\_\_\_\_.  
a. whenever a flip flop sets to 1, the next higher FF faces race condition  
b. whenever a flip flop sets to 0, the next higher FF remains unchanged  
c. whenever a flip flop sets to 1, the next higher FF toggles  
d. whenever a flip flop sets to 0, the next higher FF faces race condition

12. Which of the following expression is **CORRECT** for the given K-Map?

AB\CD	00	01	11	10
00	1	0	0	1
01	0	0	1	0
11	0	0	1	0
10	1	0	0	1

- a.  $A\bar{B}\bar{C} + \bar{B}\bar{D}$     b.  $A\bar{B}C + \bar{B}D$     c.  $\bar{B}CD + \bar{B}\bar{D}$     d.  $\bar{B}\bar{D} + BCD$

13. A mod-10 counter can ultimately \_\_\_\_\_.
- a. divide the clock frequency by 10      b. divide the clock frequency by 32  
c. divide the clock frequency by 16      d. multiply the clock frequency by 10
14. Which of these flip-flop cannot be used to constructs a serial shift register?
- a. D-flip flop      b. JK-flip flop  
c. T-flip flop      d. SR-flip flop
15. If there are 8 unused states in a counter, it must be a \_\_\_\_\_.
- a. 6 bit ring counter      b. 4 bit Johnson counter  
c. 4 bit ring counter      d. 6 bit twisted ring counter
16. The hexadecimal number  $(3E8)_{16}$  is equal to decimal number \_\_\_\_\_.
- a. 323      b. 982      c. 768      d. 1000
17. The excess-3 code of decimal 9 is represented by \_\_\_\_\_.
- a. 1100      b. 1011      c. 0101      d. 0110
18. An overflow occurs in \_\_\_\_\_.
- a. Middle position    b. MSB position    c. LSB position    d. Never occurs
19. Consider the representation of six-bit numbers by 2's complement, 1's complement, or by sign magnitude. In which representation is there overflow from the addition of the integers 011000 and 011000?
- a. 2's complement only  
b. sign magnitude and 1's complement only  
c. 2's complement and 1's complement only  
d. All three representations
20. A  $32 \times 8$  ROM consists of \_\_\_\_\_ respectively.
- a. 6 OR gates and one  $5 \times 32$  decoder      b. 32 OR gates and one  $5 \times 32$  decoder  
c. 8 OR gates and a  $4 \times 16$  decoder      d. 8 OR gates and one  $5 \times 32$  decoder

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Level : B.E./B.Sc.  
Year : II  
Time : 2 hrs. 30 mins.

Course : EEG 202  
Semester : I  
F. M. : 40

SECTION "B"  
[4Q. × 10 = 40 marks]

Attempt *ANY FOUR* questions.

1.
  - a. Implement a full-subtractor with two half-subtractors and an OR gate. [4]
  - b. Simplify the Boolean function: [4]
    - i.  $F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$
    - ii. Draw circuit using NAND Gates.
  - c. Perform the subtraction using 10's and 9's complement for  $3570 - 2100$ . [2]
  
2.
  - a. Design a mod-6 synchronous down counter and explain the operation using the timing diagram. [5]
  - b. Design a combinational logic circuit to activate and inactivate a pump in a control system where four sensors are used to operate the pump. The sensors outputs are represented by w, x, y and z. The pump is activated for the following conditions: [5]
    - i. If w is off, the remaining outputs x, y, z are on.
    - ii. If z is off, the remaining three sensors output are on
    - iii. The pump is activated if all four sensors are active.
  
3.
  - a. Design a combinational logic circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. [5]
  - b. Reduce the following state diagram shown in Figure 1. [5]

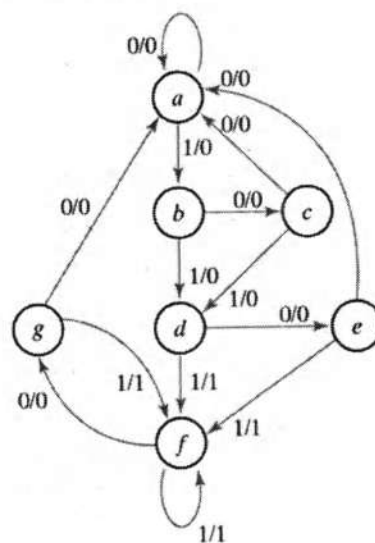


Figure 1

4.

- a. Differentiate between the multiplexer and the demultiplexer. Design a logic circuit for 3 to 1 multiplexer. [2+3]
- b. Design a serial adder to add two 8-bit binary number using Shift Register, Full Adder and a J-K flip flop. Explain the operation in detail. [5]

5.

- a. Differentiate between flip-flop and latch. Convert the SR flip-flop into the JK flip-flop with the help of excitation table. [2+3]
- b. Obtain a PLA program table for following Boolean expression. [5]
- i.  $F_1 = \sum(1,2,4,6,9)$
- ii.  $F_2 = \sum(0,6,9,10,11,15)$