KATHMANDU UNIVERSITY
End Semester Examination [C]
January, 2018

Marks scored:

Level : B.Sc.
Year : II
Course : EEEG 202
Semester: I
Exam Roll No. :
Time: 30 mins
F. M. : 20
Registration No.:
Date : JAN 12 2018

SECTION "A"
[20 × 1=20 marks]

Choose the most appropriate option. **Symbols** have their usual meaning.

1. The NOR gate output will be high if the two inputs are _____
   a. 0 0 b. 01 c. 10 d. 11

2. Which of the following expression is correct for the given K-Map?

AB\CD	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	0	0	0	1
10	1	0	0	1

   a. $\bar{B}\,\bar{C} + \bar{B}\,\bar{D}$ b. $A\,\bar{C} + \bar{B}\,\bar{D}$ c. $C\,\bar{D} + A\,\bar{B}\,\bar{C}$ d. $C\,\bar{D} + A\,\bar{B}\,\bar{D}$

3. The number of control lines for a 16 – to – 1 multiplexer is _____
   a. 2 b. 3 c. 4 d. 5

4. How many flip-flops are required for mod–12 counter?
   a. 6 b. 5 c. 4 d. 3

5. The binary equivalent of gray code 10011 is _____
   a. 11100 b. 11001 c. 10001 d. 11101

6. The simplified expression for the following expression, Y = AB+AC+BD+CD is given by
   a. (A+D) (B+C) b. (A. D) (B + C) c. (A+ $\bar{D}$) (B.C) d. (A+D) (B.C)

7. The digital logic family which has minimum power dissipation is _____
   a. TTL b. RTL c. DTL d. CMOS

8. Which of the following is universal gate?
   a. X-OR b. X- NOR c. OR d. NOR

9. A combinational circuit which converts binary information from n input lines to a maximum of 2^n unique output lines is known as _____
   a. Encoder b. Decoder c. Multiplexer d. Demultiplexer

10. The device which changes data from parallel to serial is known as _____
    a. Encoder b. Decoder c. Multiplexer d. Demultiplexer

11. A 4 bit counter counts up to _____
    a. 4 b. 3 c. 15 d. 16

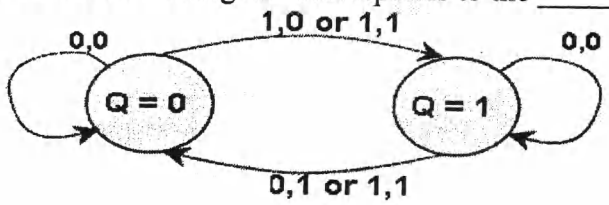
12. Which of the following expression represents the DeMorgan's law?
a. $\overline{A+B} = \overline{A} + \overline{B}$ b. $\overline{A+B} = A + B$ c. $\overline{A+B} = A.B$ d. $\overline{A+B} = \overline{A}.\overline{B}$

13. Which of the following Hexadecimal number corresponds to the binary number 10110001101011.11110010?
a. $(C6B.E2)_{16}$ b. $(3C6B.F2)_{16}$ c. $(2C5B.E2)_{16}$ d. $(2C6B.F2)_{16}$

14. For JK flip flop with J=0, K=1, the output after clock pulse will be _____
a. Low b. High c. No change d. Invalid

15. The excess-3 code of decimal 9 is represented by
a. 1001 b. 1011 c. 0101 d. 1100

16. The state transition diagram corresponds to the _____flip-flop.



a. SR flip-flop b. JK flip-flop c. D flip-flop d. T flip-flop

17. Which of the following gate can be used to construct a SR latch?
a. X-OR b. X-NOR c. NOT d. NOR

18. The characteristic equation for the JK flip flop is given by
a. Q(next) = JQ' + K'Q
b. Q(next) = JQ + K'Q
c. Q(next) = JQ' + KQ
d. Q(next) = J'Q' + K'Q

19. A 5 bit parallel input serial output shift register requires _____
a. 5 SR flip flops b. 5 JK flip flops c. 5 D flip flops d. 5 T flip flops

20. Internal logic of ROM includes_____
a. Array of AND gates
b. Array of OR gates
c. AND gates and a decoder
d. OR gates and a decoder

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Semester: I
F. M. : 55

SECTION "B"
[5 Q.× 11 = 55 marks]

Attempt *ANY FIVE* questions. Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable. Symbols have their usual meanings.

1.
a) Define radix, binary logic and Boolean algebra. How is binary logic different than arithmetic logic? [2]
b) Which gates are called as the universal gates? What are its advantages? [2]
c) Explain the design procedure for combinational circuit. [2]
d) What is the function of enable input in a multiplexer? Construct a logic circuit for 4 to 1 multiplexer. [1+4]

2.
a) What are called don't care conditions? Simplify the following Boolean function using K-map
$F(w,x,y,z) = \sum(1,3,7,11,15)$ which has the don't care conditions
$d(w,x,y,z) = \sum(0,2,5)$ [1+3]
b) Design logic circuit for BCD adder by using 4 bit binary adders. [5]
c) Why is it necessary to use tabulation method for simplifying Boolean expressions instead of K-map? Justify your answer. [2]

3.
a) Why is carry lookahead generator important? Draw logic circuit for carry lookahead generator with the help of generalized expression for carry propagation. [2+4]
b) Design a three bit synchronous counter and explain the operation with the help of time diagram. [5]

4.
a) Why is code conversion important? Draw the K-maps for BCD to excess-3 code converter and construct the logic diagram for BCD to excess-3 code converter. [1+4]
b) Construct a 5 to 32 line decoder with four 3 to 8 line decodes with enable and 2 to 4 line decoder. Use block diagram for components. [3]
c) Implement the following Boolean functions using PLA
$F_1(A,B,C) = \sum(0,1,2,4)$ and $F_2(A,B,C) = \sum(0,5,6,7)$ [3]

5.
a) Draw the characteristic table and excitation table for JK flip-flop and convert the JK flip-flop into T flip-flop with the help of excitation table. How does JK flip-flop avoid the race condition observed in SR flip-flop? [6]
b) Write the applications of shift registers. Draw logic circuit for bidirectional shift registers and also explain the operation in detail. [1+4]

6.

a) Why asynchronous counters are also known as ripple counter? Differentiate between synchronous and asynchronous counter and design a logic circuit for three bit asynchronous up/down counter. [5]

b) Derive the state table and the state diagram for the following sequential circuit as shown in figure (a) where x, y represent the input, output respectively and A, B represent states of the flip-flops. [6]

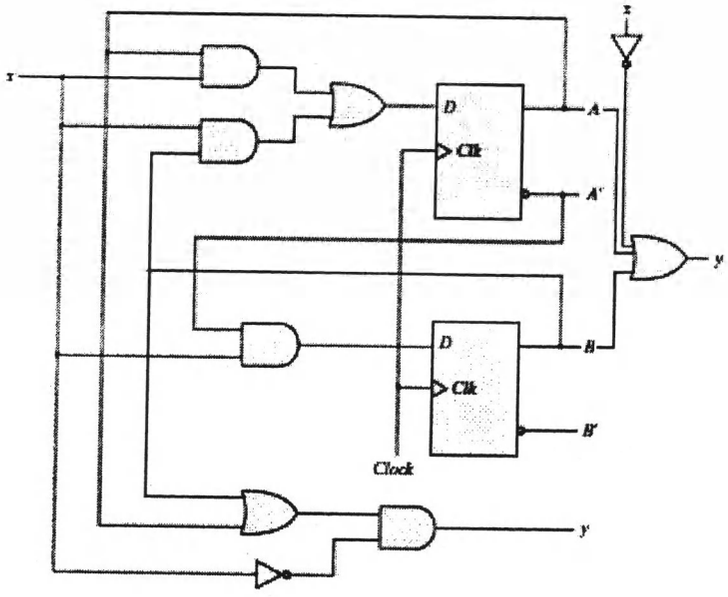

Figure (a)