Marks Scored:

KATHMANDU UNIVERSITY
End Semester Examination
February/March, 2019

Level: B.E./B.Sc. Course : EEEG 202
Year : II Semester: I

Exam Roll No. : Time: 30 mins. F. M. : 20

Registration No.: Date : FEB 2 2 2019

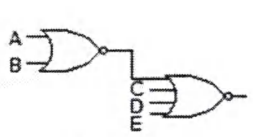
SECTION "A"
[20 Q × 1 = 20 marks]

Encircle the most suitable answer to the following questions. Calculators are not allowed.

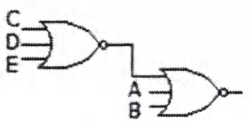
1. The output of a NOR gate is equivalent to _____.
   [a] NAND gate followed by an inverter [b] OR gate followed by an inverter
   [c] AND gate followed by an inverter [d] NOR gate followed by an inverter

2. An active high OR gate is equivalent to active low _____.
   [a] AND gate [b] NOR gate [c] NAND gate [d] X-OR gate

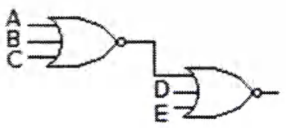
3. Implementing the expression X= [A' B' +(C + D + E)]' with NOR logic, we get:



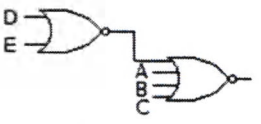
(A)



(B)



(C)



(D)

   [a] (A) [b] (B) [c] (C) [d] (D)

4. The function F = ab+bc'+ac gives the same output as that of
   i) ac+bc'
   ii) (b+c) (a+c')
   iii) (a'+c')(b'+c)
   iv) (a+c)(b+c')
   [a] i only [b] iii only [c] i and ii [d] i and iii

5. The expression F= A'+B'+C' is equivalent to which single gate?
   [a] NAND [b] NOR [c] OR [d] AND

6. $(935)_{12}$ is equivalent to _____.
   [a] $(1337)_{10}$ [b] $(2470)_8$ [c] $(10111000110)_2$ [d] $(2480)_8$

7. _____ is represented by the following figure.

[a] SR flip-flop with A = S and B = R [b] JK flip-flop with A = K and B = J
[c] A JK flip-flop with A = J and B = K [d] SR flip-flop with A = R and B = S

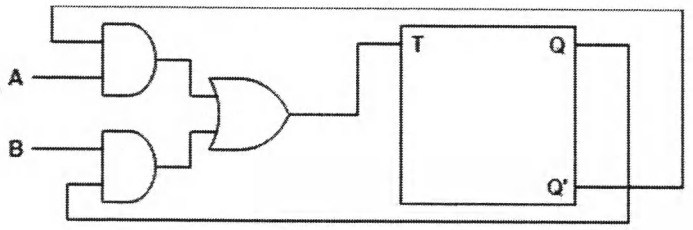


Figure 1

8. The binary representation of BCD number 00101001 is _____.

[a] 0011101 [b] 0110101 [c]1101001 [d] 0101011

9. If $(100111001)_2$ is 2's complement number, it is equivalent in decimal as _____.

[a]199 [b] -199 [c] 313 [d] -313

10. If there are 52 unused states in a counter, it must be a _____.

[a] 6 bit ring counter [b] 12 bit johnson counter
[c] 12 bit ring counter [d] 6 bit twisted ring counter

11. Flip-Flops can be constructed with two _____

[a] XOR gates [b] NAND gates [c] AND gates [d] NOT gates

12. A mod-20 counter can ultimately _____.

[a] divide the clock frequency by 20 [b] divide the clock frequency by 32
[c] divide the clock frequency by 16 [d] multiply the clock frequency by 16

13. An eight bit serial in/serial out shift register is used with a clock frequency of 2 MHz to achieve a time delay of _____.

[a] 4 µsec [b] 2 µsec [c] 0.5 µsec [d] 1 µsec

14. _____ chooses single line from multiple lines and directs the binary data to the output line.

[a] Data selector [b] Data distributor [c] Decoder [d] Encoder

15. The initial state of MOD -16 down counter is 0110. After 37 clock pulses, the state of the counter will be _____.

[a] 1011 [b] 0110 [c] 0101 [d] 0001

16. The normal output of D latch _____.
[a] follows the input when EN is low [b] complements the input when EN is high
[c] follows the input regardless of EN [d] follows the input when EN is high

17. Code is a symbolic representation of _____.
[a] continuous signal [b] discrete signal
[c] binary information into decimal [d] decimal information into binary

18. The circuit shown in Figure 2 realizes the function _____.
[a] (A'+B')C +(DE)' [b] A'+B'+C'+D'+E'
[c] AB+C(D+E) [d] AB+C+DE

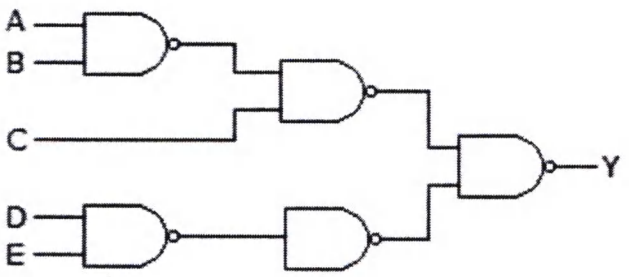


Figure 2

19. Which of the following is not equivalent to X' ?
[a] X NAND X [b] X NOR X [c] X NAND 1 [d] X NOR 1

20. The functional difference between SR and JK flip flop is _____.
[a] JK flip-flop has a feedback path
[b] JK flip-flop requires no external clock
[c] JK flip flop is faster than SR flip flop
[d] JK flip flop can accept both inputs

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SECTION "B"
[5Q × 11 = 55 marks]

Attempt *ANY FIVE* questions.

1. a. What do you mean by self-complementing codes? Explain with suitable examples. [2]
   b. Perform the following operations using 2's complement. Explain whether there is overflow in each case. [5]
      i. Subtract $(-50)_{10}$ from $(+100)_{10}$
      ii. Add $(-85)_{10}$ to $(-97)_{10}$
   c. Define timing diagram for combinational logic gates? Explain three input NOR gate with timing diagram. [4]

2. a. Find (r-1)'s complement of $(1001.001)_2$ and $(27.95)_{10}$. [2]
   b. Construct an 8×1 multiplexer using 2×1 multiplexer. [4]
   c. Design a combinational logic circuit with 4 inputs and 4 outputs that converts a 4 bit gray code into equivalent excess-3 code. [5]

3. a. Design a BCD adder. [5]
   b. Implement following functions using decoder. [4]
      F1 = (A+B'+C) (B+C+D')
      F2 = (A+B+C') (A+D)
   c. Explain the significance of priority encoder. [2]

4. a. Differentiate between characteristic table and excitation table? Obtain the characteristic table and characteristic equation for negative edge triggered S'R' flip flop. [1+4]
   b. Design a 4 bit synchronous up counter which displays even decimal number in binary format. [6]

5. a. Compare counters and registers. Design a mod -12 asynchronous down counter. [2+4]
   b. Explain how a universal register can be used as different types of registers. [5]

6. a. Design a sequential logic circuit that has 2 D flip flops and 2 inputs A and B. If A = 0, the circuit remains in the same state regardless the value of B. When A = 1 and B = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and repeats. When A = 1 and B = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and repeats. [5]
   b. Write short notes on the following. [2+2+2]
      i. Weighted binary code
      ii. Applications of shift register
      iii. Programmable logic array