KATHMANDU UNIVERSITY
End Semester Examination
February/March, 2018

Marks Scored:

Level : B.E.
Year : II

Course : EEEG 202
Semester: I

Exam Roll No.: Time : 30 mins. F.M. : 20

Registration No: Date MAR 0 4 2018

SECTION "A"
[20 Q.×1=20 marks]

Encircle the most suitable answer to the following questions:

1. Minimum number of two input NAND gates used to perform the function of two input OR gate is _____.
a) one b) two c) three d) four

2. _____ will give the sum of full adders as output.
a) Three point majority circuit b) Three bit parity checker
c) Three bit comparator d) Three bit counter

3. The number of half adder/s and full adder/s required to add two 16 bit binary numbers only is _____.
a) 8 half-adders, 16 full-adders b) 1 half-adder, 15 full-adders
c) 16 half-adders, 0 full-adder d) 4 half-adders, 12 full-adders

4. The EXCLUSIVE NOR gate is equivalent to _____ gate followed by an inverter.
a) OR b) AND c) NAND d) XOR

5. _____ shows the logical state of a digital circuit output for every possible combination of logical states in the inputs.
a) Routing table b) Function table c) Truth table d) ASCII table

6. A demultiplexer is used to _____.
a) route the data from single input to one of many outputs
b) perform serial to parallel conversion
c) select data from several inputs and route it to single output
d) encode the signal

7. _____is the minimum number of 2 input NAND gates required to implement the function $F = (x' + y')(z + w)$.
a) 6 b) 5 c) 4 d) 3

8. _____ are best suited for 'parity' checking and 'parity' generation.
a) AND, OR, NOT gates b) EX-NOR or EX-OR gates
c) NAND gates d) NOR gates

9. _____ can add three or more numbers at a time.
a) Parallel adder
b) Carry look ahead adder
c) Carry save adder
d) Full adder

10. A small dot or circle printed on top of an IC indicates _____.
a) Vcc
b) GND
c) Pin 14
d) Pin 1

11. The full adder adds the Kth bits of two numbers to the _____.
a) difference of the previous bits
b) sum of all previous bits
c) carry from $(K - 1)^{th}$ bit
d) sum of previous bit

12. The SR, JK and D inputs are called _____.
a) Asynchronous inputs
b) Synchronous inputs
c) Synchronous outputs
d) Asynchronous outputs

13. Four JK flip-flops are cascaded with their JK inputs tied HIGH. If the input frequency (fin) to the first flip flop is 32 kHz, the output waveform is _____.
a) 2 kHz square wave
b) a 32 kHz square wave
c) a constant low
d) a constant high

14. Initially a 4 bit shift left register is in 1001 state. If the serial input 1011010 is applied, Take leftmost bit is the first bit to enter into the flip-flop, _____ will be the state of register after 4 left shift?
a) 1010
b) 0110
c) 1011
d) 1001

15. A 5 bit Johnson counter has _____ states.
a) 5
b) 10
c) 15
d) 20

16. According to Boolean law: A + 1 = _____.
a) 1
b) A
c) 0
d) A'

17. An overflow occurs in _____
a) MSB position
b) LSB position
c) Middle position
d) Never occurs

18. On subtracting 010110 from 1011001 using 2's complements, we get _____.
a) 0111001
b) 1000011
c) 0110110
d) 0101100

19. The decimal equivalent of the excess-3 number 110010100011.01110101 is _____.
a) 970.42
b) 1253.75
c) 861.75
d) 12.45

20. The pictorial representation of truth table is called a _____.
a) Venn diagram
b) Karnaugh Map
c) Graphical map
d) Tabular Map

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SECTION "B"

- ✓ *Attempt any FIVE questions*
- ✓ *Assume any suitable data if necessary*
- ✓ *Figures in margin indicate full marks for each questions*

1)

a) What is the use of error detection codes during transmission? Explain with suitable examples. [3]

b) Represent the decimal number 8620 (i) in BCD, (ii) in excess-3 code, (iii) in 2421 code [3]

c) What is the difference between canonical form and standard form? Convert the following to the other canonical form [5]

$$F = w'xz + w'yz + x'yz' + wxy'z$$
$$d = wyz$$

2)

a) What are the constraints to be considered during a practical design method? [2]

b) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output line that generate the 9's complement of the input digit. [5]

c) Explain encoder? Design a circuit that compares two 4-bit numbers, A and B, to check if they are equal. The circuit has one output x, so that x = 1 if A = B and x = 0 if A ≠B. [1+3]

3)

a) How can decoder be used as a demultiplexer? Explain with necessary tables/figures [3]

b) Implement a full-adder circuit with multiplexers. [4]

c) Consider a JK' flip flop and obtain the flip-flop characteristics table and its characteristics equation. [4]

4)

a) A sequential circuit has two flip-flops (A and B), two inputs (x and y), and an output (z). The flip flop input functions and the circuit output functions are as follows: [6]

$$JA = xB + y'B'$$
$$KA = xy'B'$$
$$JB = xA'$$
$$KB = xy' + A$$
$$z = xyA + x'y'B$$

Obtain the logic diagram, state table, state diagram, and state equations.

b) Explain types of registers? Design a 4 bit asynchronous binary up down counter. [5]

5)

a) What is the difference between serial and parallel transfer? What type of register is used in each case? [5]

b) Design a synchronous BCD counter with JK flip flops. [6]

6)

a) Define latch and flip-flop. Convert T flip flop to SR flip flop [5]

b) Write short notes on: [2+2+2]
   i) Fan Out
   ii) Digital Computer
   iii) Counters