KATHMANDU UNIVERSITY
End Semester Examination [C]
December, 2024

Level : B.E./B.Sc.
Year : II
Time : 2 hrs. 30mins.

17 DEC 2024

Course : EEEG 202
Semester : I
F. M. : 40

SECTION "B"
[4 Q. × 10 = 40 marks]

Attempt ANY FOUR questions. Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable. Calculators are not allowed.

1.
a. Differentiate between the standard form and the Canonical form of Boolean expression and minimize the following Boolean function using K-Map: [1+4]
F (A, B, C, D) = $M_4 M_6 M_4 M_{11} M_{14} M_{15}$
b. Using 10's complement, perform the following subtraction: [2]
$(470 - 231)_{10}$
c. Write truth table and design logic circuit for 3-bit binary to Gray code converter. [3]

2.
a. Design a combinational circuit using a ROM. The circuit accepts a three-bit number andoutputs a binary number equal to the square of the input number. [5]
b. Design a logic circuit for 3 bit asynchronous up/down counter and explain the working mechanism with the help of timing diagram. [5]

3.
a. Derive the characteristic equation of T flip-flop and convert the T flip-flop into SR flip-flop with the help of excitation table. [2+3]
b. How does parity bit method help to detect the error? Design a logic circuit for even parity checker for 3-bit message and discuss the limitation of this method. [5]

4.
a. Design a logic circuit having four inputs W, X, Y, Z whose output is high whenever both Y and Z are high as long as W and X are either both low or both high. [5]
b. Write short notes on: [2.5x2]
i. Johnson counter
ii. Edge triggered flip-flop

5.
a. Explain the working of universal shift register with the help of circuit diagram. [4]
b. Design a sequential logic circuit specified by the state diagram of **figure1** using T flip-flop. [6]

P.T.O.

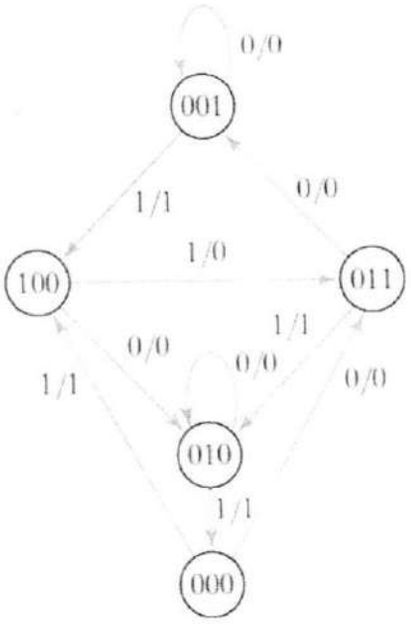

Figure1