KATHMANDU UNIVERSITY
End Semester Examination
August/September, 2017

Marks scored:

Level : B.Sc.
Year : II

Course : EEEG 202
Semester: I

Exam Roll No. :

Time: 30 mins

F. M. : 20

Registration No.:

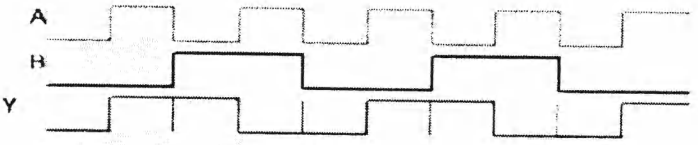
Date :

SECTION "A"
[20Q × 1 = 20 marks]

Choose the most appropriate option. Symbols have their usual meaning.

1. The binary equivalent of decimal number 0.625 is .....
   a. 0.101 b. 0.110 c. 0.111 d. 0.100

2. If A and B are inputs to a two input logic gate and Y is the output of the gate then which of the gate corresponds to the following output waveform?



   a. AND b. OR c. X-OR d. X-NOR

3. If A and B are inputs to the two input X-OR gate, which of the following expression for output is correct?
   a. $\bar{A}B + A\bar{B}$ b. $\bar{A}\bar{B} + A\bar{B}$ c. $\bar{A}B - A\bar{B}$ d. $\bar{A}\bar{B} + AB$

4. Which of the following Boolean postulate is true?
   a. $X + X = 2X$ b. $X + X = 0$ c. $X + X = 1$ d. $X + X = X$

5. Which of the following represents the DeMorgan's law?
   a. $\overline{A+B} = \bar{A} + \bar{B}$ b. $\overline{A+B} = A + B$ c. $\overline{A+B} = A.B$ d. $\overline{A+B} = \bar{A}.\bar{B}$

6. 10's complement of decimal number 012398 is given by
   a. 12398 b. 02231 c. 32154 d. 033216

7. Which of the following expression represents the Boolean function F = A +B'C in sum of min terms
   a. $F(A,B,C) = \sum(0,2,3,4,5)$ b. $F(A,B,C) = \sum(1,4,5,6,7)$
   c. $F(A,B,C) = \sum(1,3,5,6,7)$ d. $F(A,B,C) = \sum(2,4,5,6,7)$

8. Which of the following is universal gate?
   a. AND b. OR c. AND d. NOR

9. Which of the following binary combination represents the result of BCD addition of two BCD numbers 1000 and 1001?
   a. 10001 b. 01110 c. 10111 d. 10110

10. A ROM internally includes programmable ..... gates and a decoder.
    a. AND b. OR c. X-OR d. NOR

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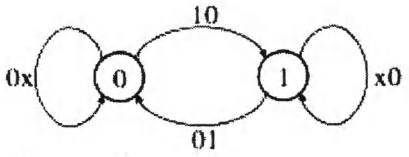
11. Flip flop conversion expressions for JK flip flop to D flip flop are given by
a. J = D, K = D b. J = $\overline{D}$, K = D c. J = D, K = 1 d. J = D, K = $\overline{D}$

12. The characteristic equation for the T flip flop is given by
a. Q(t+1) = T$\overline{Q}$ + $\overline{T}$ Q
b. Q(t+1) = T$\overline{Q}$ + TQ
c. Q(t+1) = Q$\overline{T}$ + $\overline{T}$ Q
d. Q(t+1) = $\overline{T}$ $\overline{Q}$ + TQ

13. The following figure represents the state transition diagram of .....



a. SR flip-flop b. D flip-flop c. T flip-flop d. JK flip-flop

14. For JK flip flop with J=1, K=0, the output after clock pulse will be
a. Low b. High c. No change d. Complimented

15. While implementing a Boolean function having N variables, the number of selection lines for a multiplexer is equal to
a. N b. N^2 c. 2N d. N-1

16. A N bit synchronous up counter counts up to .....
a. N b. N^2 c. 2N d. N-1

17. Mod-10 asynchronous up counter requires ..... flip flops.
a. 10 b. 5 c. 4 d. 3

18. Which of the following expression is correct for the given K-Map?

AB\CD	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	1	0	0	0
10	1	0	0	0

a. F = $\overline{C}$ $\overline{D}$ + $\overline{A}$ C b. F = $\overline{C}$ $\overline{D}$ + $\overline{A}$ $\overline{C}$ c. F = $\overline{C}$ $\overline{D}$ + AC d. F = C D + $\overline{A}$ $\overline{C}$

19. BCD input 0000 is fed to a seven segment display through BCD to seven segment decoder/driver. The segments which will lit up are:
a. a,b,d,e,f b. a,b,c ,d,e,f c. all d. a,b,c,d,f,g

20. A 4 bit serial input serial output shift register requires .....
a. 4 SR flip -flops b. 4 JK flip- flops c. 4 D flip- flops d. 4 T flip- flops

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SECTION "B"

[5 Q.× 11 = 55 marks]

Attempt *ANY FIVE* questions. Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable.

1.
   a. How does a NAND gate act as Universal gate? Explain with suitable figures. [3]
   b. Perform the subtraction on the following unsigned binary numbers using the 2's complement of the subtrahend. (a) 11011 – 11001 (b) 101010 – 101011 [3]
   c. Describe the working of serial in parallel out shift register with circuit diagram and timing diagram. [5]

2.
   a. Simplify the following Boolean function using K-map
      $F(w,x,y,z) = \sum(1,3,7,11,15)$ which has the don't care conditions
      $d(w,x,y,z) = \sum(0,2,5)$ [4]
   b. Implement the following Boolean function with NOR gate [2]
      $F(x,y,z) = (1,2,3,4,5,7)$
   c. Design logic circuit for BCD adder by using 4 bit binary adder. [5]

3.
   a. Implement the following 4-input Boolean function with a Multiplexer
      $F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$ [3]
   b. Design logic circuit for 3 bit binary to gray code converter. [3]
   c. Write the truth table for 4-input priority encoder and draw logic circuit for 4-input priority encoder. [5]

4.
   a. Design a logic circuit that has four inputs A, B, C, D and an output that is to be high only when input A is high and at the same time other two inputs are also high. [4]
   b. Draw the state transition diagram of JK flip-flop and explain the working of master-slave JK flip-flop? [1+3]
   c. Implement the following Boolean functions using PLA
      $F_1(A,B,C) = \sum(0,1,2,4)$ and $F_2(A,B,C) = \sum(0,5,6,7)$ [3]

5.
   a. Design a logic circuit for mod-6 synchronous down counter and explain the operation using timing diagram. [5]
   b. Draw the characteristic table and excitation table for SR flip-flop. Is it possible to avoid the race condition occurred in SR flip-flop? Justify your answer. [4]
   c. Differentiate between the Mealy and Moore sequential circuits with examples. [2]

6.

a. Design a logic circuit for mod-12 asynchronous up counter and explain the operation using timing diagram. [5]

b. Draw the state table and state diagram of the following synchronous sequential circuit (Figure 1) where x represents the input and A, B represent the states of the flip-flops. [6]

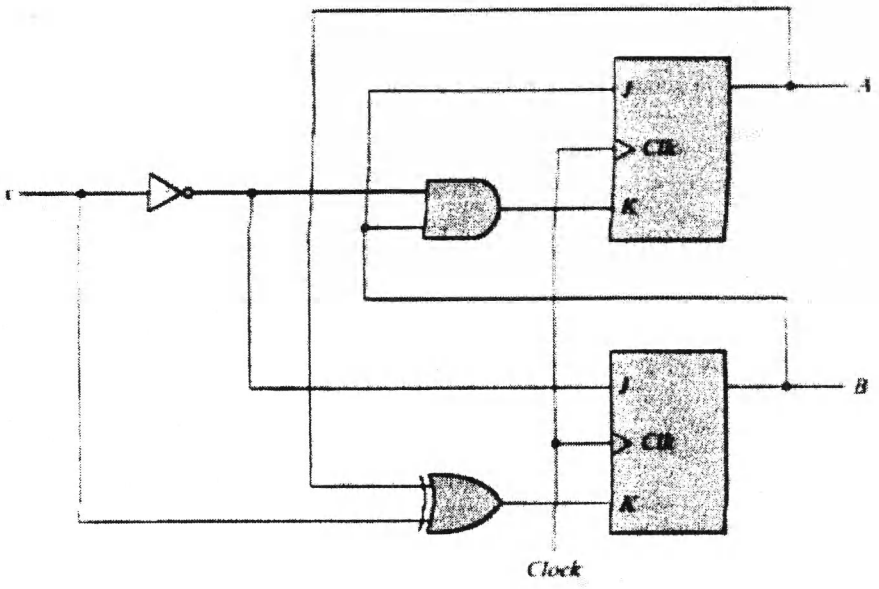

Figure 1