KATHMANDU UNIVERSITY
End Semester Examination [C]
April/May, 2023

Marks Scored:

Level : B.E.
Year : II

Course : EEEG 202
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date : 27 APR 2023

SECTION "A"
[20Q. × 0.5 = 10 marks]

Encircle the most appropriate option. **Symbols** have their usual meaning.

1. The number of OR gates required for the implementation of Boolean functions using ROM for the following functions is _____.
$F_1(a,b,c) = \sum m(0,1,3,6,7)$ and $F_2(a,b,c) = \sum m(3,5,6,7)$
a. 1 b. 2 c. 3 d. 4

2. Which of the following device can be used as parallel to serial convertor?
a. Multiplexer b. Demultiplexer c. Encoder d. Decoder

3. How many flip-flops are required for mod–6 counter?
a. 6 b. 5 c. 4 d. 3

4. How many 3×8 decoders are required to construct a 4×16 decoder?
a. 4 b. 3 c. 2 d. 1

5. A 4 to 2 encoder requires _____ logic gates.
a. 1 b. 2 c. 3 d. 4

6. The digital logic family which has minimum power dissipation is _____.
a. TTL b. RTL c. DTL d. CMOS

7. Which of the following expression is correct for the given K-Map?

Table 1

AB\CD	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	1	1	0	0
10	1	1	0	0

a. $F = \bar{C}\,\bar{D}$ b. $F = \bar{A}\,\bar{C}$ c. $F = \bar{C}$ d. $F = \bar{D}$

8. Which of the following logic gate can be used as a one-bit magnitude comparator?
a. AND b. OR c. NOT d. X-OR

9. A $(1010.011)_2$ is equal to _____.
a. $(15.975)_{10}$ b. $(8.75)_{10}$ c. $(13.57)_{10}$ d. $(10.375)_{10}$

10. Which of the following expression represents the DeMorgan's law?
a. $\overline{A+B} = \overline{A} + \overline{B}$ b. $\overline{A+B} = A + B$ c. $\overline{A+B} = A.B$ d. $\overline{A+B} = \overline{A}.\overline{B}$

11. Which of the following Hexadecimal number corresponds to the binary number $1011110001100110.10101111_2$?
a. $(BC6B.EA)_{16}$ b. $(BC6B.F)_{16}$ c. $(BC5B.E2)_{16}$ d. $(BC66.AF)_{16}$

12. For JK flip flop with J=1, K=1, the output after clock pulse will be _____.
a. Low b. High c. Complimented d. Invalid

13. What would be the gray code equivalent to the decimal number 14?
a. 1000 b. 1110 c. 1001 d. 1111

14. BCD input 0000 is fed to a seven segment display through BCD to seven segment decoder/driver. The segments which will lit up are _____.
a. a, b, d, e, f b. a, b, c, d, e, f c. a, b, c, d, f, g d. all

15. Figure 1 represents the circuit of _____ .
a. Synchronous counter
b. Asynchronous counter
c. Ring counter
d. Combinational circuit

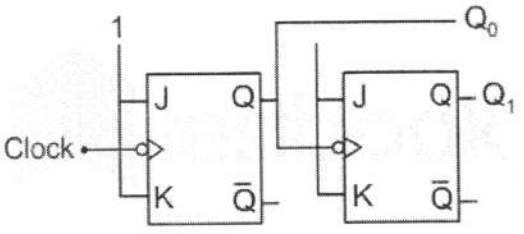

Figure 1

16. The state transition diagram in Figure 2 corresponds to the _____flip-flop.

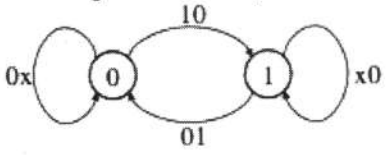

Figure 2

a. SR flip-flop b. JK flip-flop c. D flip-flop d. T flip-flop

17. A N bit synchronous up counter counts up to _____.
a. N b. 2^N c. $2^N - 1$ d. N-1

18. The characteristic equation for the T flip flop is given by
a. $Q(next) = T \oplus Q$ b. $Q(next) = T \oplus Q'$
c. $Q(next) = T' \oplus Q$ d. $Q(next) = T' \oplus Q'$

19. A 4-bit parallel input serial output shift register requires _____.
a. 4 SR flip flops b. 4 JK flip flops c. 4 D flip flops d. 4 T flip flops

20. Which of the following is **TRUE** in case of Moore sequential logic circuit?
a. Output depends on current input
b. Output depends on current state
c. Output depends on previous output
d. Output depends on current input and current state

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SECTION "B"
[4Q. × 10 = 40 marks]

Attempt *ANY FOUR* questions. Symbols have their usual meanings.

1.

a. What are called don't care conditions? Simplify the following Boolean function using K-map.
$F(w,x,y,z) = \sum(1,3,7,11,15)$ which has the don't care conditions
$d(w,x,y,z) = \sum(0,2,5)$ [1+4]

b. Design a logic circuit that has four inputs w, x, y, z and an output that is to be high only when input z is low and at the same time other two inputs are also high. [5]

2.

a. Design a logic circuit for carry lookahead generator with the help of generalized expressions for carry propagation. [5]

b. Design a sequential circuit with two D flip-flops A and B, and one input x. when x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transition from 00 to 01 to 11 to 10 back to 00, and repeats. [5]

3.

a. How is binary logic different from arithmetic logic in Boolean algebra? Explain with examples. [3]

b. Construct a 5 to 32-line decoder with four 3 to 8 line decodes with enable and 2 to 4-line decoder. Use block diagram for components. [3]

c. Implement the following Boolean functions using ROM. [4]
$F_1(A, B, C) = \sum (0,1,2,4)$ and $F_2(A, B, C) = \sum (0,5,6,7)$

4.

a. How does a mod-6 synchronous up counter work? Explain the operation using a suitable logic circuit. [6]

b. Explain the characteristics of Mealy and Moore circuit with the help of example. [4]

5.

a. Design a logic circuit for three bit asynchronous up/down counter and explain the operation with the help of timing diagram. [4]

b. Draw the logic circuit for 3-bit universal shift register and explain the working mechanism in detail. [6]