KATHMANDU UNIVERSITY
End Semester Examination
February/March, 2018

Marks Scored:

Level : B.E.
Year : III
Course : EEEG 314
Semester: I
Exam.Roll No.:
Time: 30 mins.
F.M. : 20
Registration No.:
Date : FEB 26 2018

SECTION "A"
[20 Q.×1=20 marks]

Encircle the most suitable answer to the following questions:

1) _____ is not a vectored interrupt.
a) TRAP b) INTR c) RST 7.5 d) RST 3.

2) Basic Steps of execution of an instruction is _____.
a) Fetch → Execute → Decode
b) Decode → Fetch → Execute
c) Execute → Fetch → Decode
d) Fetch → Decode → Execute

3) _____ happens when RET instruction is executed by any subroutine.
a) The top of the stack will be popped out and assigned to PC
b) Without any operation, the calling program would resume from instruction immediately following the call instruction
c) Without any operation, the calling program would resume from instruction immediately following the call instruction and also the PC will be incremented after the execution of the instruction.
d) The PC will be incremented after the execution of the instruction

4) _____ T-states are required for execution of OUT 80H instruction.
a) 10 b) 13 c) 16 d) 7

5) _____ is the length of instruction POP D
a) 1 Byte b) 2 Byte c) 3 Byte d) 4 Byte

6) Microprocessor comprises of _____.
a) Register Section b) Control Unit c) ALU d) All

7) _____ while INX B instruction is executed
a) Only carry flag will be affected
b) all flags will be affected
c) only carry and zero flags will be affected
d) no flags will be affected

8) A microprocessor with a 12-bit address bus will be able to access _____ bytes.
a) 1 K b) 4 K c) 8 K d) 10 K

9) Data storage in stack is designed in _____ method.
a) FIFO b) LILO c) FILO d) LIFO

10) _____ stands for PSW.
a) accumulator contents b) flag byte
c) accumulator and flag contents d) none

11) Which among these memory types cannot be re-written after once.
a) PROM b) EPROM c) EEPROM d) EAROM

12) The contents of the A15 – A8 while executing IN 8-bit port address instruction are _____.
a) irrelevant b) all bits reset
c) all bits set d) same as content of A7 – A0

13) _____ of the interrupts are only level triggering.
a) TRAP b) RST 7.5
c) RST 6.5 and RST 5.5 d) RST 6.5

14) The stack is a set of reserved _____.
a) ROM address space b) RAM address space
c) I/O space d) none

15) S0 and S1 pins are used for _____.
a) serial communication b) indicating the processor status
c) acknowledging the interrupt d) stack operation

16) _____ is the vector address of INTR.
a) 0024 H b) 003C H c) 0034 H d) no address

17) _____ after the execution of CMP A instruction
a) Z flag is set and CY flag is reset
b) Z flag is set and CY flag is unchanged
c) Z flag is reset and CY flag is set
d) Z flag is reset and CY flag is unchanged

18) _____ is an 8085 hardware interrupt.
a) TRAP b) RST 6.5 c) RST 7.5 d) all of the above

19) Address line for RST3 is _____.
a) 0020H b) 0028H c) 0018H d) 0010H

20) The stack pointer resides in _____.
a) RAM b) ROM c) Microprocessor d) RAM or ROM

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FEB 2 6 2018

Level : B.E.
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Time : 2 hrs. 30 mins.

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F.M. : 5 5

SECTION "B"

- ✓ *Attempt any FIVE questions*
- ✓ *Assume any suitable data if necessary*
- ✓ *Figures in margin indicate full marks for each questions*

1. a) Explain the 8085 programming Model with figure. [4]

   b) What do you understand by de-multiplexing and what is the need of de-multiplexing the bus$AD_7 - AD_0$. [4]

   c) Differentiate between partial and absolute decoding with example. [3]

2.a) Design an input and output interfacing circuit with address FFH and FEH respectively. Connect two switches in input port D_0 *and* D_1 and LEDs on the output port. Write instructions to read the input port and continue to read it until both switches are closed. When both the switches are closed, turn on all the LEDS. [5]

   b) Explain memory-mapped I/O and peripheral mapped I/O technique with example. [2]

   c) Write a program to load data byte 8EH in register D and F7H in register E. Mask the higher-order bits $(D_7 - D_4)$ from the data bytes. Exclusive OR the lower order bits $(D_3 - D_0)$, and display the answer in PORT 01H. [4]

3.a) Explain the flow process of RET instruction. What is the difference between JMP and CALL instructions? [3+1=4]

   b) Design a counter with 1ms delay with register pair. Include calculations and program. [3]

   c) Define SIM and RIM instructions with interpretations of its bit pattern? [4]

4.a) Explain operation of interfacing an 8-bit A/D converter using a status check. [3]

   b) Convert an analog input voltage of 0.43 V into 8 bit digital output. Consider 1V as a Full scale voltage. [3]

c) Design an interfacing circuit to meet the following requirement. [5]
   i) 74LS138: 3 to 8 decoder
   ii) 2732 (4K x 8): EPROM – address range should begin at 0000H and additional 4K memory space should be available for future expansion.
   iii) 6116 (2K x 8) : CMOS R/W memory

5.a) Design a square wave generator with a pulse width of 100us by using the 8155 timer. Set up the timer in Mode 1 if the clock frequency is 3MHz. [6]

b) Draw the timing waveforms of I/O port of 8155 in handshake mode for both INPUT and OUTPUT mode. [5]

6.a) How does data flow from memory to the microprocessor? Explain in detail with bus timings? [5]

b) A set of three packed BCD numbers (six digits) representing time and temperature are stored in memory locations starting at XX50H. The seven-segment codes of the digits 0 to 9 for a common-cathode LED are stored in memory locations starting at XX70H, and the Output Buffer memory reserved at XX90H. Write a program and subroutines to unpack the BCD numbers and select an appropriate seven-segment code for each digit. **(Flow chart is mandatory)** [6]