KATHMANDU UNIVERSITY
End Semester Examination
March/April, 2017

APR 6 2017

Level : B.E./B. Sc.
Year : III
Time : 2 hrs. 30 mins.

Course : COMP 315
Semester : I
F. M. : 40

SECTION "B"
[6Q × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. How can you perform addition and subtraction of fixed point numbers in 2's complement form? Illustrate with example for each case.

2. Design an arithmetic circuit with one selection variable S and two n–bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram of first 3 MSB's.

S	$C_{in} = 0$	$C_{in} = 1$
0	D= A – 1 (Decrement)	D = A+ B' + 1 (Subtract)
1	D = A+B (Add)	D = A+ 1 (Increment)

3. Discuss daisy-chain method of priority interrupt handling.
OR
Discuss the working principle of 4×4 FIFO Buffer.

4. What do you mean by stack organization? What are the major difference between register stack and memory stack?

5. Briefly discuss set associative mapping used in cache memory organization.

6. Multiply 4 bits magnitude value by 4 bits magnitude value using array multiplier. Illustrate with figure if necessary. Discard sign bits for both multiplicand and multiplier.

7. With flowchart and necessary RTLs, discuss instruction execution process during instruction cycle.

SECTION "C"
[2Q × 8 = 16 marks]

Attempt *ANY TWO* questions.

8. Discuss the characteristics of RISC processor. Divide [-48] by [+9] for signed magnitude data. [4+4=8]

9. Discuss DMA transfer process with necessary figure(s). What are the things to be considered while using arithmetic shift left and shift right operations? Illustrate with some examples. [4+2+2=8]

10. Describe how read and write operations are performed in Random Access Memory with suitable block diagram? Explain BSA and ISZ instructions with necessary RTL's for execution cycle only. Draw the block diagram and describe the operation for the hardware that implements the following statements: [2+3+3=8]

$x + yz$: **AR ←AR + BR**

Where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function.