Marks scored:

KATHMANDU UNIVERSITY
End Semester Examination
March/April, 2017

Level : B.E./B. Sc.
Year : III
Course : COMP 315
Semester : I
Exam. Roll No. :
Time: 30 mins.
F. M. : 10
Registration No.:
Date : APR 6 2017

SECTION "A"
[20 Q × 0.5 = 10 marks]

Tick (√) the correct answer(s).

1. What is the name of an address in main memory?
[ ] Physical address [ ] Logical address [ ] Memory address [ ] Word address

2. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be
[ ] $(812)_{10}$ [ ] $(-12)_{10}$ [ ] $(12)_{10}$ [ ] $(-812)_{10}$

3. Which register keeps tracks of the instructions stored in program stored in memory?
[ ] AR (Address Register) [ ] XR (Index Register)
[ ] PC (Program Counter) [ ] AC (Accumulator)

4. In a vectored interrupt.
[ ] the branch address is assigned to a fixed location in memory.
[ ] the interrupting source supplies the branch information to the processor through an interrupt vector.
[ ] the branch address is obtained from a register in the processor
[ ] none of the above

5. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be
[ ]11 bits [ ] 21 bits [ ] 16 bits [ ] 20 bits

6. What is the 2's compliment form (Use 6 bit word) of the number 1010?
[ ]111100 [ ]110110 [ ]110111 [ ]101100

7. What is the content of Stack Pointer (SP)?
[ ] Address of the current instruction [ ] Address of the next instruction
[ ] Address of the top element of the stack [ ] Size of the stack.

8. Memory access in RISC architecture is limited to instructions
[ ] CALL and RET [ ] PUSH and POP [ ] STA and LDA [ ] MOV and JMP

9. Considering each integer number is used as 8 bit number, the sum of -6 and -13 using 2's complement addition is,
[ ]11100011 [ ]11110011 [ ]11001100 [ ]11101101

10. An instruction cycle refers to
[ ] Fetching an instruction
[ ] Decoding an instruction
[ ] Fetching, decoding and executing an instruction
[ ] Executing and instruction

11. What is the 4-bit Gray code of $(17)_{10}$? _____
[ ]11101 [ ]11001 [ ]10111 [ ]11110

12. What should be the size of multiplexer for constructing a common bus with k registers of n bits each using multiplexer?
[ ] k × 1 [ ] (k+1) × 1 [ ] n× 1 [ ] (n+1) × 1

13. In Branch Unconditional instruction, the RTL at the execution cycle at T4 is
[ ] D_6T_4: PC←AR [ ] D_6T_4: DR←M [AR]
[ ] D_6T_4:DR←M [MAR] [ ] D_6T_4: M [AR] ← AC

14. On a Karnaugh map, grouping the 0s produces
[ ] a "don't care condition" [ ] a sum-of-products expression
[ ] AND-OR logic [ ] a product-of-sums expression

15. Memory mapped I/O involves transferring of
[ ] Information between memory locations [ ] Information between I/O devices and CPU
[ ] Information among CPU registers [ ] Information between CPU and Memory

16. _____is concerned with the way the hardware components operate to form computer system.
[ ] Computer organization [ ] Computer design
[ ] Computer architecture [ ] Computer implementation

17. When the control function $\mathbf{D_7IT_3 = 1}$, which operation will be executed by the basic computer?
[ ] Execute register-reference instruction [ ] AR ← M [AR]
[ ] Execute input-output instruction [ ] No operation

18. What is true regarding RISC?
a. Relatively few instructions
b. Single-cycle instruction execution
c. Micro-programmed
d. Fixed length
[ ] a & b & c [ ] a & c & d [ ] a & b & d [ ] b & c & d

19. The load instruction is mostly used to designate a transfer from memory to a processor register known as _____
[ ] Accumulator [ ] Instruction Register
[ ] Data Register [ ] Temporary Register

20. A Program Counter contains a number 825 and address part of the instruction contains the number 24.Assume an instruction is a 1 byte instruction. What is the effective address in the relative address mode, when an instruction is read from the memory ?
[ ] 849 [ ] 850 [ ] 801 [ ] 802