KATHMANDU UNIVERSITY
End Semester Examination [C]
June, 2018

Marks Scored:

Level : B.E./B.Sc.
Year : III

Course : COMP 315
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date : JUN 18 2018

SECTION "A"
[20 Q. × 0.5 = 10 marks]

Tick (√) the correct answer(s).

1. In memory-mapped I/O…
   [ ] The I/O devices and the memory share the same address space
   [ ] The I/O devices have a separate address space
   [ ] The memory and I/O devices have an associated address space
   [ ] A part of the memory is specifically set aside for the I/O operation

2. The method of accessing the I/O devices by repeatedly checking the status flags is
   [ ] Memory-mapped I/O [ ] I/O mapped
   [ ] Program-controlled I/O [ ] DMA

3. In case of Zero-address instruction method, the operands are stored in _____ .
   [ ] Registers [ ] Accumulators [ ] stack [ ] Cache

4. The register that keeps track of the instructions in the program stored in memory is …...
   [ ] Accumulator [ ] Program counter
   [ ] temporary register [ ] Instruction register

5. The device which is used to connect a peripheral to bus is called
   [ ] Control register [ ] Communication protocol
   [ ] decoder [ ] Interface

6. In a vectored interrupt, ……
   [ ] the branch address is assigned to a fixed location in memory.
   [ ] the interrupting source supplies the branch information to the processor through an interrupt vector.
   [ ] the branch address is obtained from a register in the processor
   [ ] the branch address is not available

7. Which shift is a shift micro operation which is used to shift a signed binary number to the left or right:
   [ ] Logical [ ] Circular [ ] rotate [ ] Arithmetic

8. For a 2 bytes instruction, a Program Counter contains a number 700 and address part of the instruction contains the number 24. The effective address in the PC relative address mode, when an instruction is read from the memory is
   [ ] 724 [ ] 725 [ ] 726 [ ] 700

9. In Branch and save return address (BSA) instruction, the RTL at the execution cycle at T4 is
   [ ] D_5T_4: DR←M [AR], AR←AR+1 [ ] D_5T_4: PC←AR, AR←AR+1
   [ ] D_5T_4: M [AR] ←PC, AR←AR+1 [ ] D_5T_4: M [AR] ←AC, AR←AR+1

10. In an unsigned multiplication algorithm, if the least significant bit of multiplier is 0, then what operation will you perform?
[ ] Addition [ ] Subtraction
[ ] Arithmetic shift right [ ] Logical shift right

11. In binary division the sign of the remainder is same as the sign of .....
[ ] quotient [ ] dividend [ ] divisor [ ] sequence counter

12. What is the content of Stack Pointer (SP)?
[ ] Address of the current instruction [ ] Address of the next instruction
[ ] Address of the top element of the stack [ ] Size of the stack

13. In daisy chaining method of interrupt handing, devices are connected in..... manner.
[ ] Parallel [ ] Random [ ] Serial [ ] Synchronous

14. What is the 1's complement of 0000 1111 0010 1101 number?
[ ] 1111 0000 0010 1101 [ ] 1111 0000 1101 0010
[ ] 1111 1100 1010 1100 [ ] 1001 0010 1010 1100

15. $(FA)_{16}$ is the _____ one's complement representation of -5.
[ ] 4-bit [ ] 8-bit [ ] 16-bit [ ] 2-bit

16. A NAND gate has inputs A and B. It's output is connected to the both of the inputs of another NAND gate. An equivalent gate for these two NAND gates is
[ ] OR gate [ ] AND gate [ ] NOR gate [ ] XOR gate

17. In daisy chaining method device with PI=.....and PO=.....is the one with higher priority that is requesting an interrupt
[ ] 1, 0 [ ] 0, 1 [ ] 1, 1 [ ] 0, 0

18. Cache memory works on the principle of
[ ] Locality of data [ ] Locality of reference
[ ] Locality of memory [ ] Locality of reference & memory

19. Which of the following is not a weighted code?
[ ] Decimal Number system [ ] Excess 3-code
[ ] 2421 code [ ] 84-2-1 code

20. An adder-subtractor single unit can be designed using full adder and
[ ] OR gates [ ] XOR gates [ ] NOR gates [ ] NAND gates

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SECTION "B"
[6Q × 4 = 24 marks]

Attempt *ALL* questions.

1. Differentiate between computer organization and computer architecture? Describe about different types of ROMs? [2+2]

2. Design a 5-bit arithmetic circuit that is capable of performing addition, subtraction, increment, decrement, and transfer operations. Show the function table for this arithmetic circuit. [4]

3. Describe Instruction cycle of Load Accumulator (LDA) instruction with necessary Register transfer language. Assume direct addressing is used in instruction to load the data.

4. Discuss interrupt handling method for Parallel Priority Interrupt. [4]

5. Multiply (-7) * (-5) using Booth's algorithm. With a block diagram, briefly explain hardware requirements. [3+1]

6. Design a combination circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2, 3 the output is one greater than the input. When the binary input is 4, 5, 6, 7 the output is always one less than the input.

SECTION "C"
[2Q × 8 =16 marks]

Attempt *ALL* questions.

7. Discuss shift micro-operations with examples. Draw the block diagram of parity generator and parity checker for 3 bits data using odd parity. [4+4]

8. Compare register stack organization and memory stack organization. Draw flowchart for multiplication algorithm for signed magnitude data. [4+4]