KATHMANDU UNIVERSITY
End Semester Examination
July/August, 2024

Level : B.E/B.Sc.
Year : III
Time : 2 hrs. 30mins.

13 AUG 2024

Course : COMP 315
Semester : I
F. M. : 50

SECTION "B"
[6 Q. × 4 = 24 marks]

Attempt ANY SIX questions.

1. With a neat diagram discuss the concept of parity generator and parity checker. Write down the binary table for the 2421 code and 84-2-1 code. [2+2]

2. Illustrate the importance of ASHR and ASHL operations. Briefly discuss their working mechanisms with an example. List out the application of logical shift micro-operations.

3. Design a Common Bus System (CBS) to connect four 8-bit registers using the multiplexer. Verify it using Tri-State Buffer.

4. Illustrate the working mechanism of the block diagram shown in Figure 1 considering a typical **Input/output** instruction.

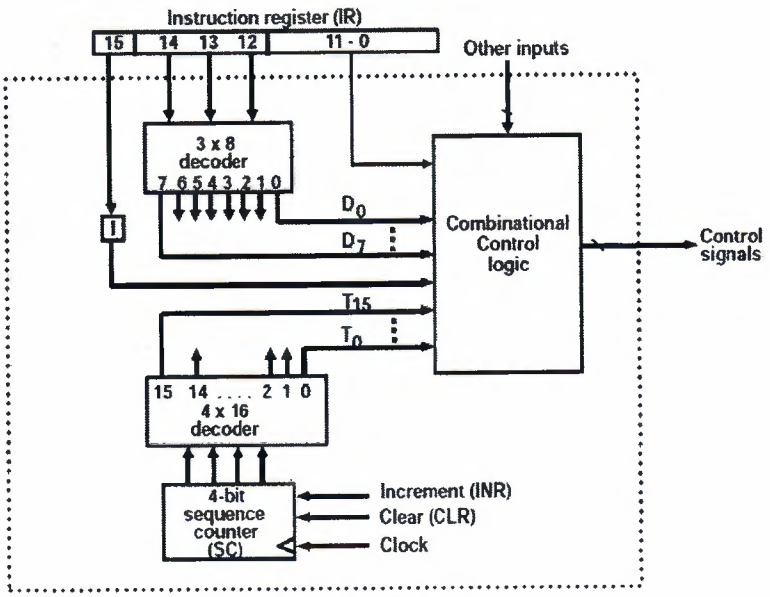

Figure 1: Block diagram of a unit

5. Discuss the sequence of micro-operations for two instructions, 0 LDA 255 and 1 AND 245, stored in RAM at memory locations 23 and 24 respectively, with an initial PC value of 23, referring to the instruction cycle and Register Transfer Language, assuming all necessary data.

6. With a necessary diagram, discuss the working mechanism of a general register organization-based Central Processing Unit. What are the pros and cons of this organization? [2+2]

P.T.O.

7. With the necessary figure, discuss the Direct Memory Access I/O data transfer technique.

SECTION "C"

[2 Q. × 8 = 16 marks]

Attempt ANY TWO questions.

8. Illustrate the role of the interrupt cycle in computer architecture. Design the PC and ALU of a Basic Computer based on the data given in Table 5_6. [2+3+3]

9. Draw the flowchart for the **Booth's** approach to multiplication. Divide (+277) by (-19) using a restoring division method. Also, check for overflow. [3+4+1]

10. List the various addressing modes used by a Central Processing Unit, and discuss auto-increment and auto-decrement modes with typical scenarios, as well as provide details on relative addressing modes. What is a processor status register and what is the purpose of using it in a CPU? [2+2+2+2]

TABLE 5-6 Control Functions and Microoperations for the Basic Computer

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$, $AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	D_7IT_3:	$AR \leftarrow M[AR]$
Interrupt:		
	$T_0'T_1'T_2'(IEN)(FGI + FGO)$:	$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$
Register-reference:		
		$D_7I'T_3 = r$ (common to all register-reference instructions)
		$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$
	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow$ shr AC, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow$ shl AC, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$
Input-output:		
		$D_7IT_3 = p$ (common to all input-output instructions)
		$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$
	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$

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Registration No.:

Date :

SECTION "A"

[20 Q. × 0.5 = 10 marks]

Choose and mark [X] in the most appropriate option:

1. The logical expression AB + A'B' can be implemented by using 2-input:
   [ ] NOR gate [ ] XNOR gate [ ] NAND gate [ ] XOR gate

2. The decimal number (-34) is expressed in 2's complement form as _____.
   [ ] 01011110 [ ] 10100010 [ ] 11011110 [ ] 01011101

3. Floating point representation is used to store
   [ ] Boolean values [ ] whole numbers [ ] real integers [ ] integers

4. In Basic Computers, the instruction is recognized as MRI or RRI, or IoI _____
   [ ] at T_0 cycle [ ] at T_1 cycle [ ] at T_2 cycle [ ] after T_2 cycle

5. The correct sequence of a data hierarchy in ascending order is:
   [ ] bit - bytes - record - field - file - database
   [ ] bit - bytes - fields - record - file – database
   [ ] bytes - bit- field - record - file - database
   [ ] bytes -bit - record - field - file – database

6. How can you apply a decrement operation for data that has an 8-bit value?
   [ ] By adding eights 1's in the original value and discarding the carry
   [ ] By subtracting eight 1's in the original value
   [ ] First, add eight 1's in the original value then subtract
   [ ] decrement operation cannot be implemented

7. The addressing mode that identifies a register holding the memory address of the operand is:
   [ ] Indirect Addressing Mode
   [ ] Register Addressing Mode
   [ ] Register Indirect Addressing Mode
   [ ] Base Address Register Addressing Mode

8. In Branch and Save Return Address (BSA) instruction, the RTL expression at the T_4 cycle is
   [ ] D_5T_4: DR←M [AR], AR←AR+1 [ ] D_5T_4: PC←AR, AR←AR+1
   [ ] D_5T_4: M [AR] ←PC, AR←AR+1 [ ] D_5T_4: M [AR] ←AC, AR←AR+1

9. The infix expression (A / B * C + D) has reverse polish notation equivalent to
   [ ] A B / C * D + [ ] A B C * / D + [ ] A B C / D + * [ ] A B C / * D +

10. In the daisy chaining method of interrupt handing, devices are connected in_____ manner.
[ ] Parallel [ ] Random [ ] Serial [ ] Synchronous

11. A stack organized computer use _____ addressing.
[ ] Indexed [ ] one [ ] Two [ ] zero

12. To multiply (5) * (9) excluding sign bits for both multiplier and multiplicand, we need _____ AND gates and _____'s parallel adder of _____ bits.
[ ] 12, 3, 3 [ ] 12, 4, 3 [ ] 9, 4, 3 [ ] 9, 3, 4

13. Consider the two 8-bit numbers A=01000001 and B=10000100 represented in 2's complement form. Performing COMPARE B, A yields _____
[ ] Branch if Positive [ ] Branch if Overflow
[ ] Branch if Carry [ ] No option

14. The _____ Micro-operation checks equality between two numbers and the logical gate used is _____
[ ] Selective Clear, X- OR [ ] Selective Complement, X - OR
[ ] Compare, X – NOR [ ] Compare, X-OR

15. To design a Common Bus System for four registers having eight bits each, we need
[ ] 8 MUX, 4* 1Size, 2 selection lines [ ] 8 MUX, 8*1 size, 3 selection lines
[ ] 4 MUX, 8*1 size, 3 selection lines [ ] 4 MUX, 4*1 size, 2 selection lines

16. Register R contains the binary value 10011100. What will be the value after the arithmetic shift right?
[ ] 01001110 [ ] 11001110 [ ] 00111000 [ ] 00111001

17. What is true regarding RISC?
a. Relatively few instructions
b. Single-cycle instruction execution
c. Micro-programmed
d. Fixed length

[ ] a & b & c [ ] a & c & d [ ] a & b & d [ ] b & c & d

18. During the DMA acknowledgment cycle, CPU relinquishes _____.
[ ] Control, status, data output, data input
[ ] Data input, data output, status, control
[ ] Control, flag, data output, address
[ ] Data input, data output, status bit, address

19. In basic computer instruction formats, if an op-code field contains 010, it is a/an _____instruction.
[ ] AND [ ] LDA [ ] ADD [ ] BSA

20. What DVF is calculated by _____ in the Restoring-Division algorithm?
[ ] ADDING B and checking the value of E
[ ] Subtracting B and checking the value of E
[ ] Checking the value of E before subtracting
[ ] Checking the value of E before adding