KATHMANDU UNIVERSITY
End Semester Examination [C]
June/July 2024

Level : B.E/B.Sc.
Year : III
Time : 2 hrs. 30 mins.

04 JUL 2024

Course : COMP 315
Semester : I
F.M. : 40

SECTION "B"
[6Q. × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. Differentiate between Computer Architecture and Computer organzation? Describe about four different types of ROM? [2+2=4]

2. What is the drawback with BCD? How it can be overcome by certain weighted code, describe it with example? Perform the arithmetic operation (-82)10 + (-5)10 using signed-2's complement representation? [2+2=4]

3. Design an arithmetic circuit with one selection variable S and two n–bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram of first 2 MSB's.

S	Cin = 0	Cin = 1
1	D= A – 1 (Decrement)	D = A+ B' + 1 (Subtract)
0	D = A+B (Add)	D = A+ 1 (Increment)

4. As a computer designer, when will you say that an instruction set of a computer is complete? Design a common bus for a basic computer with single accumulator organization, which has 8 registers [DR(16 bit), AR(12 bit), AC(18bit), IR(18 bit), PC(12 bit), TR(18 bit), INPR(8 bit), OUTR(8 bit)], a memory unit(4096×16) and Adder and logic unit with overflow flag(E), this ALU has 3 sets of input (AC, DR and INPR) and output to AC? Explain why the given microoperation **(IR←M[PC])** cannot execute during the single clock pulse in the system with above common bus configuration. Specify the sequence of microperations that will perform the operation [1+2+1=4]

5. An expression is needed to be converted into program. Write three address, two address, one address and zero address instruction for the given expression. [1+1+1+1=4]
   X= (A * B – C + D / E) * G / H

6. Discuss handshaking method for asynchronous data transfer. Draw the block diagram of 2 * 3 FIFO Buffer. [2+2=4]

7. What do you mean by page fault? Describe Two-way set-associative Mapping of Cache Memory with suitable example? [1+3=4]

P.T.O.

SECTION "C"

[2Q. × 8 = 16 marks]

Attempt *ANY TWO* questions.

8. Draw a flowchart for showing addition and subtraction process for two fixed-point binary numbers where these numbers are represented in signed-2's complement form ? Show the step-by-step multiplication process using Booth's algorithm for performing $(-12)_{10} \times (-15)_{10}$. [3+5=8]

9. Differentiate between Asynchronous and synchronous serial data transfer? Explain three different possible modes that are used for transferring data to and from peripherals? [2+6=8]

10. For the given questions use the Control functions and Microoperations for the Basic Computer given in next page.
    a. Derive the control gates for the write input of the memory in the basic computer? [3]
    b. Show the complete logic of the interrupt flip flop 'R' in the basic computer. Use JK flip flop and minimize the number of gates? [5]

KATHMANDU UNIVERSITY
End Semester Examination [C]
June/July 2024

Marks Scored:

Level : B.E./B.Sc.
Year : III
Course : COMP 315
Semester : I

Exam Roll No. :
Time: 30 mins.
F. M. : 10

Registration No.:
Date 04 JUL 2024

SECTION "A"
[20Q. × 0.5 = 10 marks]

Choose and mark [X] in the most appropriate option from each set of choices

1. On a Karnaugh map, grouping the 0s produces
   [ ] a product-of-sums expression
   [ ] a sum-of-products expression
   [ ] a "don't care condition"
   [ ] AND-OR logic

2. When an inverter is placed between both inputs of an SR flip flop, the resulting flip flop is
   [ ] JK flip flop
   [ ] T flip flop
   [ ] D flip flop
   [ ] Master slave JK flip flop

3. Which memory is used for storing our documents in a mobile phone?
   [ ] ROM [ ] PROM [ ] EPROM [ ] EEPROM

4. Which device is used for Parallel to serial conversion of data?
   [ ] Multiplexer [ ] Decoder [ ] Encoder [ ] Register

5. What is the 2's complement form of $(-34)_{10}$?
   [ ] 01011110 [ ] 10100010 [ ] 11011110 [ ] 01011101

6. The 4 bit odd parity generator circuit consists of
   [ ] 2 X-OR gates, 1 X-NOR gate
   [ ] 1 X-OR gates, 2X-NOR gate
   [ ] 3 X-OR gates
   [ ] 3 X-NOR gate

7. How many decoders are required to construct a common bus for **k** registers of **n** bits each using 3-state buffers?
   [ ] k [ ] k+1 [ ] n [ ] n+1

8. What is the operation that sets to 1 the bits in one register where there is corresponding 1's in the second register?
   [ ] Selective clear
   [ ] Selective Complement
   [ ] Selective set
   [ ] Insert

9. To execute the RTL statement $\mathbf{R'T_0}$: **AR←PC,** Which line of PC should go high?
   [ ] Clear [ ] Increment [ ] Load [ ] Clock

10. When the control function $\mathbf{D_7'IT_3 = 1}$, which operation will be executed by the basic computer?
    [ ] Execute register-reference instruction
    [ ] Execute input-output instruction
    [ ] AR ← M [AR]
    [ ] Nothing

11. Convert the expression (A+B) *[C*(D+E)+F] from infix to reverse polish notation
    [ ] AB+CDE*+F+*
    [ ] AB+CDE+*F+*
    [ ] AB+CDE*+F*+
    [ ] AB+DE+C*F+*

12. Which addressing Mode doesn't use any memory reference to obtain an Operand?
[ ] Direct [ ] Indirect [ ] Immediate [ ] Register Indirect

13. In an unsigned binary division algorithm after performing a subtraction operation, how can we identify whether the obtained value is negative or not?
[ ] Carry in and carry out of MSB is same
[ ] Carry out of MSB is 1
[ ] Carry in and carry out of MSB is different
[ ] Borrow out of MSB is 1

14. In 2's complement multiplication algorithm, if the value of least significant bit in register holding Multiplier is 1 and register $\mathbf{Q}_{-1}$ is 0, then what operation will you perform?
a. $A \leftarrow A - M$
b. $A \leftarrow A + M$
c. Arithmetic shift right
d. Logical shift right
[ ] a & c [ ] b & c [ ] c only [ ] b & d

15. In which I/O communication method does the CPU continuously check the status of an I/O device?
[ ] Interrupt-driven I/O [ ] Direct Memory Access (DMA)
[ ] Direct Memory Access (DMA) [ ] Programmed I/O

16. "Seek a given record on a magnetic disk", the given command belongs to
[ ] Control command [ ] Status command
[ ] Data input command [ ] Logical command

17. What is the main purpose of Direct Memory Access (DMA)?
[ ] To allow the CPU to communicate directly with memory
[ ] To transfer data between memory and I/O devices without CPU intervention
[ ] To handle interrupts from I/O devices
[ ] To increase the clock speed of the CPU

18. What is/are **TRUE** regarding Direct Mapping in cache memory organization?
a. Inexpensive
b. Fastest and most flexible
c. Index field is used for the address to access the cache
[ ] a & b [ ] a & c [ ] b & c [ ] a & b & c

19. How many 128 × 8 RAM chips are needed to provide a memory capacity of 1024 bytes?
[ ] 1 [ ] 4 [ ] 8 [ ] 2

20. What is the typical characteristic of memory as you move down the memory hierarchy from registers to secondary storage?
[ ] Increased speed and cost [ ] Decreased speed and increased cost
[ ] Decreased speed and cost [ ] Increased speed and decreased cost