

10. What is represented by $D_7 I' T_3$ in the instruction cycle?
 Register – Reference Instructions Program Interrupt
 Input-Output Instructions Memory Reference Instructions
11. How many 128×8 RAM chips are needed to provide a memory capacity of 1024×16 bytes?
 1 16 8 2
12. In multiplication algorithm using Signed Magnitude Representation, if the value at Q_n after SHR 0, then what operation will you perform?
 Addition Subtraction
 Arithmetic shift right No change in previous state
13. How many decoders are required to construct a common bus for k registers of n bits each using 3-state buffers?
 k $k+1$ n $n+1$
14. In basic computer instruction formats, if op-code field contains 111, it is instruction.
a. Memory-reference instructions b. Register-reference instructions
c. Input-output instructions
 a. only b. only c. only both b & c
15. The representation of $(-17)_{10}$ in ANSI 32-bit floating point numbers in byte format will be
 00000101 10001000 00000000 00000000
 10000100 01000100 00000000 00000000
 10001011 10001000 00000000 00000000
 10000101 10001000 00000000 00000000
16. Consider the two 8-bit numbers $A=01000001$ and $B=10000100$. Add the two binary numbers assuming that the numbers are represented in 2's complement form. After performing add operation which conditional branch instruction will have true condition?
 Branch if Zero Branch if overflow
 Branch if minus Branch if carry
17. On a Karnaugh map, grouping the 0s produces
 a product-of-sums expression a "don't care condition"
 a sum-of-products expression AND-OR logic
18. In Reverse Polish notation, expression $A * B + C * D$ is written as
 $AB * CD * +$ $A * B CD * +$ $AB * CD + *$ $A * B * CD +$
19. $T: R2 \leftarrow R1, R1 \leftarrow R2$
Which statement is true regarding above micro operation?
 There are three micro operations in a single clock pulse
 There are two micro operations in a single clock pulse
 There is one micro operation in a single clock pulse
 This is invalid operation
20. A hand-shake based protocol for data transfer is an example of _____ type of data transfer.
 Synchronous Asynchronous Serial Indirect

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F. M. : 40

SECTION "B"

[6Q × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. What is asynchronous data transfer? How can you ensure the reliability in asynchronous data transfer between peripheral and CPU? Briefly discuss any two methods. [1+3]
2. Describe the Three addresses, 2 addresses, one address and zero address instruction formats with typical example. [4]
3. Multiply $[+8] * [-12]$ using Booth's algorithm. [4]
4. Branch and Save return address (BSA) is hardware implementation of function call. Illustrate its instruction cycle with necessary Register Transfer Language. [4]
5. How can we check overflow during addition of two numbers using signed 2's complement representation? Briefly explain the self complementary code. [2+2]
6. A 6-bit register contains the binary value 110010. What is the register value after arithmetic shift right? Draw the block diagram and describe the operation for the hardware that implements the following statements:
$$x + y z: \quad AR \leftarrow AR + BR$$
Where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function. [1+3]
7. A digital computer has a memory unit of $64K \times 16$ and cache memory of 1K words. The cache uses direct mapping with a block size of four words. [4]
 - a. How many bits are there in the tag, index, block, and word fields of the address format?
 - b. How many words are bits are there in each word of cache, and how are they divided into functions? Include a valid bit
 - c. How many blocks can the cache accommodate?

SECTION "C"

[2Q × 8 = 16 marks]

Attempt *ALL* questions.

8. What are the advantages of memory mapped I/O over Isolated I/O? Explain 4×4 First-In, First-out buffer with its circuit diagram? Describe Interrupt service routine in I/O management. [1+ 4+3]
9. Describe multiplication algorithm for signed magnitude representation with flowchart? Show the step-by-step division process using division algorithm for performing $(-23)_{10} / (-5)_{10}$. [4+4]

