KATHMANDU UNIVERSITY
End Semester Examination
January/February 2024

Level : B.E/B.Sc.
Year : III
Time : 2 hrs. 30 mins.

08 FEB 2024

Course : COMP 315
Semester : I
F.M. : 40

SECTION "B"
[6Q. × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. Describe Von Neumann architecture, How does it differ from Harvard Architecture? Differentiate between PROM and EEPROM? [3+1]

2. What are the drawbacks of Binary Coded Decimal? How it can be overcome by certain weighted code, describe it with example? Perform the arithmetic operation $(-82)_{10} + (-5)_{10}$ using signed-2's complement representation? [2+2]

3. Represent the following conditional control statement by two register transfer statements with control functions.
If (M=1) then (R1← R2) else if (N=1) then (R1← R3)
Design a 4-bit Combinational circuit decrementer using full –adder circuits. [1+3]

4. Branch unconditionally is an instruction used by CPU to skip certain portion of a program and jump to a label defined by user. Discuss how it is done with reference to fetch, decode and execution cycle.

5. Describe the different types of CPU organization? An instruction "LOAD" is stored at location 600 with its address field at location 601. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect [2+2]

6. What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt? Design and describe parallel priority interrupt hardware for a system with eight interrupt sources? [1+3]

7. What do you mean by page hit ratio in cache memory? Describe Direct Mapping of Cache Memory with suitable example and block diagram? [1+3]

SECTION "C"
[2Q. × 8 = 16 marks]

Attempt *ANY TWO* questions.

8. Derive an algorithm in flowchart form for adding and subtracting two fixed point binary numbers when negative numbers are in signed-1's complement representation? Divide [+105] by [-15]. Assume that numbers are signed magnitude numbers also check for divide overflow? [3+5]

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9. Write the sequence of micro-operations of basic computer along with the control function for Interrupt cycle considering interrupt flip flop? A digital computer has a memory unit with a capacity of 16, 384 words, and 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer? [2+6]

10. What are the advantages of memory mapped I/O over Isolated I/O? Explain 4 × 4 First-In, First-out buffer with its circuit diagram? Describe Destination initiated handshaking with suitable block and timing diagram? [1+5+2]

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Registration No.:

Date :

SECTION "A"

[20Q. × 0.5 = 10 marks]

Choose and mark [X] in the most appropriate option from each set of choices

1. XOR circuits can be constructed using .....
   [ ] OR gates only [ ] AND, OR gates
   [ ] AND, NOT gates [ ] AND, NOT and OR gates

2. What is a trigger pulse?
   [ ] A pulse that starts a cycle of operation
   [ ] A pulse that reverses the cycle of operation
   [ ] A pulse that prevents a cycle of operation
   [ ] A pulse that enhances a cycle of operation

3. The device used to convert a binary number to a 7-segment display format is .....
   [ ] multiplexer [ ] encoder [ ] decoder [ ] register

4. The m-bit parallel adder consists of ..... full adders.
   [ ] (m+1) [ ] m/2 [ ] m-1 [ ] m

5. The excess-3 code for 584 is.....
   [ ] 100010110111 [ ] 100001110111 [ ] 100010010110 [ ] 100001010110

6. The representation of $(-17)_{10}$ in ANSI 32-bit floating point numbers in byte format will be
   [ ] 00000101 10001000 00000000 00000000
   [ ] 10000100 01000100 00000000 00000000
   [ ] 10001011 10001000 00000000 00000000
   [ ] 10000101 10001000 00000000 00000000

7. What should be the number of tri state buffer for constructing a common bus with **k** registers of **n** bits each using tri state buffer and decoder?
   [ ] k [ ] n [ ] k+1 [ ] n × k

8. Which operation is used for performing selective –complement micro operation?
   [ ] logic-OR [ ] exclusive-OR [ ] logic-AND [ ] logic- NOT

9. In basic Computer, while designing the 16 bit common bus, the inputs to the Adder and logic units are coming from:
   a. Accumulator (AC) b. Input Register (INPR) c. Program Counter (PC)
   [ ] a & b [ ] b & c [ ] a & c [ ] a, b & c

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10. When the control function $D_7'I'T_3 = 1$, which operation will be executed by the basic computer?
[ ] Execute register-reference instruction [ ] AR ← M [AR]
[ ] Execute input-output instruction [ ] Nothing

11. Which of the following characteristics holds TRUE for RISC architecture?
a. Relatively few instructions b. Hardwired Control
c. Variable length instruction format d. Single cycle instruction execution
[ ] a, b & c [ ] b, c & d [ ] a, b & d [ ] a, c & d

12. Consider the two 8-bit numbers A=11110000 and B= 00010100. After performing **Subtract** operation which conditional branch instruction will have true condition?
[ ] Branch if Zero [ ] Branch if overflow
[ ] Branch if minus [ ] Branch if carry

13. Find the value of AVF after performing 1 011111 + 1 101101. Here leftmost bit represents the sign bit.
[ ] 0 [ ] 1 [ ] Missing Data [ ] Don't Care (×)

14. For what value of Q_n, Q_{n+1}, subtraction of AC & BR is performed in booth multiplication algorithm?
[ ] 00 [ ] 01 [ ] 10 [ ] 11

15. "Read interface status register", the given command belongs to .....
[ ] Control command [ ] Status command
[ ] Data input command [ ] Logical command

16. After the completion of the DMA transfer, the processor is notified by.....
[ ] Bus request [ ] Bus grant
[ ] DMA Acknowledgement [ ] Interrupt

17. In FIFO buffer, the two control lines, output ready and delete constitutes:
a. Source initiated pair of handshake lines
b. Destination initiated pair of handshake lines
c. Synchronous transfer
[ ] a only [ ] b only [ ] c only [ ] a & c

18. Hit ratio of cache memory defined as?
[ ] number of hits divided by total of hits plus misses
[ ] number of hits divided by number of misses
[ ] total of hits plus misses divided by number of hits
[ ] number of misses divided by number of hits

19. The main memory is 4K × 9 and cache memory is 256 × 9 in associative mapping. What is the size of argument register?
[ ] 9 bits [ ] 12 bits [ ] 6 bits [ ] 10 bits

20. How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
[ ] 2 [ ] 8 [ ] 4 [ ] 16