KATHMANDU UNIVERSITY
End Semester Examination
February/March, 2019

Mark Scored:

Level : B. E./B. Sc.
Year : III
Course : COMP 315
Semester : I
Exam Roll No. :
Time: 30 mins.
F. M. : 10
Registration No. :
Date FEB 2 4 2019

SECTION "A"
[20 Q. × 0.5 = 10 marks]

Tick (√) the correct answer(s).

1. If you compare two equal unsigned numbers A and B, If A >B then the value of flags C= ..... and Z= ..... respectively.
[ ] 0, 0 [ ] 0, 1 [ ] 1, 0 [ ] 1, 1

2. Which of the following addressing mode specifies an operand within the instruction?
[ ] Indirect Addressing Mode [ ] Register Direct Addressing Mode
[ ] Register Indirect Addressing Mode [ ] Immediate Addressing Mode

3. In Branch and save return address (BSA) instruction, the RTL at the execution cycle T_4 is
[ ] D_5T_4: DR← M [AR], AR ← AR+1 [ ] D_5T_4: PC←AR, AR ← AR+1
[ ] D_5T_4: M [AR] ← PC, AR←AR+1 [ ] D_5T_4: M [AR] ← AC, AR←AR+1

4. Suppose my instruction has 2 indirect bits, 4 op-code bits and 20 address bits, the size of RAM will be .....
[ ] 1 M * 20 [ ] 1 M * 26 [ ] 2 M * 20 [ ] 2 M * 26

5. In daisy chaining method device with PI =.....and PO =.....is the one with higher priority that is requesting an interrupt and Vector address will be ..... to CPU.
[ ] 1, 0, PASSED [ ] 0, 1, BLOCKED
[ ] 1, 1, BLOCKED [ ] 0, 0, PASSED

6. Which of the following describes the Mnemonic SNA and SZE?
[ ] Skip If (Address Resister) Negative and E flag is zero.
[ ] Skip If (Accumulator) Negative and E flag is one.
[ ] Skip If (Adder-Subtractor) Negative and E flag is zero.
[ ] Skip If (Accumulator) Negative and E flag is zero.

7. In Memory mapped I/O, the address space .....
[ ] is shared between memory and I/O devices.
[ ] used distinct location for I/O devices and memory.
[ ] is not required.
[ ] is stack.

8. To execute the RTL statement **$R'T_0$: AR←PC,** Which line of PC should go high?
[ ] Clear [ ] Increment [ ] Load [ ] Clock

9. DMA controller use ..... and ..... signals to communicate with CPU.
[ ] BR and BG [ ] INTR and INTACK
[ ] BG and BR [ ] DMAREQ and DMACK

10. J is multiplicand bits and K is multiplier bits in an array multiplier, to multiply (5) * (9) excluding sign bits, we need ..... AND gates and .....'s parallel adder of ..... bits.
[ ] J * K, K-1, J [ ] J + K, J-1, K [ ] J * K, J-1, K [ ] J + K, K-1, L

11. In multiplication algorithm for signed magnitude numbers, if the value at Q_n =1, then the operation you perform is .....
[ ] Addition of A with B then SHR [ ] Subtraction of A with B then SHR
[ ] Arithmetic Shift Right only [ ] Logical Shift Right only

12. Handshaking based method is ..... reliable than strobe and use ..... signals to communicate.
[ ] less, two [ ] more, one [ ] more, two [ ] more, one

13. What is the 2's complement representation of -24 in a hexadecimal equivalent?
[ ] $(FFFE)_{16}$ [ ] $(FFE7)_{16}$ [ ] $(0018)_{16}$ [ ] $(0017)_{16}$

14. SHR and ASHR operations are equivalent when .....
[ ] The MSB bit is zero [ ] The MSB bit is one
[ ] the number is in 2's complement [ ] the number is in 1's complement

15. Which operations are implemented using a binary counter?
[ ] Shifting [ ] logical [ ] transfer [ ] arithmetic

16. 2421 code of $(5)_{10\ is}$
[ ] 0101 [ ] 1100 [ ] 0011 [ ] 1011

17. The ..... micro-operation checks equality between two numbers and the logical gate use is .....
[ ] Compare, X-OR [ ] Selective Clear, X- OR
[ ] Selective Complement, X - OR [ ] Compare, X – NOR

18. In a 4-bit parity system, the parity output from parity generator is 1 and output from parity checker is 1, which of the following is true
[ ] System is using odd parity and transfer has some problem
[ ] System is using odd parity and transfer has no problem
[ ] System is using even parity and transfer has some problem
[ ] System is using even parity and transfer has no problem

19. In Timing and Control Unit of a Basic Computer, the size of decoder for op-code and timing unit are ..... respectively.
[ ] 3 * 8 and 3 * 8 [ ] 4 * 16 and 3 * 8
[ ] 3 *8 and 4 *16 [ ] 4 * 16 and 4 * 16

20. In Reverse Polish notation, expression A - B * C + D / E is written as
[ ] A B C * D E / - + [ ] A B – C * D + E /
[ ] A B - C * D E / + [ ] A B C * - D E / +

KATHMANDU UNIVERSITY
End Semester Examination
February/March, 2019

FEB 2 4 2019

Level : B. E./B. Sc.
Year : III
Time : 2 hrs. 30 mins.

Course : COMP 315
Semester : I
F. M. : 40

SECTION "B"
[6Q × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. Discuss the purpose of floating point representation. In what way it is different than fixed point representation. [2+2]

2. Discuss selective set, selective complement, insert and mask micro-operations as logical instructions. [1+1+1+1]

3. Discuss the working mechanism of BSA instruction with reference to fetch, decode and execute cycle. In what way it is different than interrupt? [3+1]

4. An expression is needed to be converted into program. Write three address, two address, one address and zero address instruction for the given expression. [1+1+1+1]

X= (A * B – C + D / E) * G / H

5. Draw the flowchart of Booth's algorithm and multiply (- 4) * (+ 3). [2+2]

6. Discuss handshaking method for asynchronous data transfer. Draw the block diagram of 2 * 3 FIFO Buffer. [2+2]

7. Discuss the characteristics of CISC processor. What is the purpose of end around carry in 2's complement addition? [3+1]

SECTION "C"
[2Q × 8 = 16 marks]

Attempt *ANY TWO* questions.

8. Suppose that you are dividing a value by another value. Illustrate whether division is possible or not. Divide [+75] by [-11]. Assume that numbers are signed magnitude numbers. COMPARE is an instruction use to compare two values A and B. Illustrate how can you find whether the number is greater than or less than or equal to. Assume 10101011 and 01111011 are stored as 2's complement numbers in A and B respectively. [2+3+3]

9. A **Daisy Chain** is a serial mechanism to handle priority interrupt. Discuss its working principle including the block diagram and low-level diagram to handle interrupt acknowledgement. Draw the internal diagram of common bus system for four registers each having 4 bits data. [4+4]

10. Write short notes on (*ANY FOUR*) [4 × 2 = 8]
    a. Instruction cycle
    b. Arithmetic Shift
    c. Interrupt Cycle
    d. General Register Organization
    e. Array Multiplier