

KATHMANDU UNIVERSITY
End Semester Examination
February/March, 2018

Level : B.E./B.Sc.
Year : III
Time : 2 hrs. 30 mins.

MAR 16 2018
Course : COMP 315
Semester: I
F.M. : 40

SECTION "B"
[6 Q. × 4 = 24 marks]

Attempt any SIX questions.

1. How do you check overflow in signed 1's complement numbers addition? Discuss self-complementary code with an example. [2+2]
2. Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in} . Draw the logic diagram of first 2 MSB's.

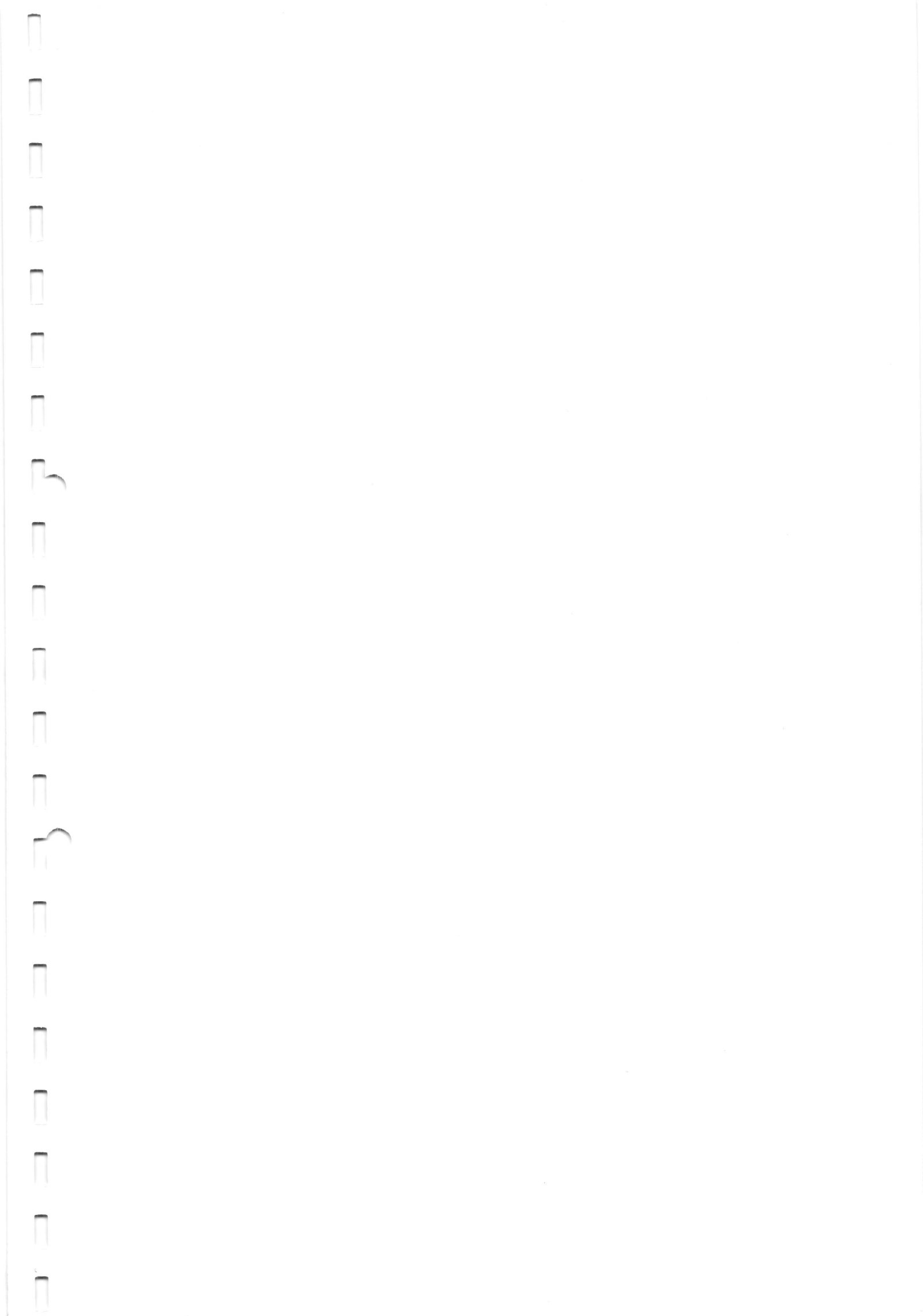
S	$C_{in} = 0$	$C_{in} = 1$
1	$D = A - 1$ (Decrement)	$D = A + B' + 1$ (Subtract)
0	$D = A + B$ (Add)	$D = A + 1$ (Increment)

3. Discuss the working principle of BSA instruction. Include the necessary RTL's statement along with the necessary figures.
4. Compare among different shifting approaches. What will be the final value when 1101011 is arithmetically shifted towards right? [3+1]
5. What is direct memory access? Describe with necessary figures. [4]
6. Discuss division algorithm with necessary flowchart. [4]
7. Discuss general register organization with necessary figure. [4]

SECTION "C"
[2 Q. × 8 = 16 marks]

Attempt any TWO questions.

8. Draw the flowchart of Booth's algorithm. Discuss the hardware requirements to implement Booth's algorithm. Multiply $(-5) * (+5)$ using Multiplication algorithm. Assume the values are signed magnitude numbers. [3+2+3]
9. With reference to the table included, design E and R flip flop of a Basic Computer. Also, design Accumulator and ALU of a Basic Computer. [2+2+2+2]
10. Represent the expression $(A / B * C) + (D - E)$ as 3 address, 2 address, 1 address and zero address instruction. Discuss interrupt cycle with necessary RTLs. [4+4]



Fetch	$R'T_0:$	$AR \leftarrow PC$
	$R'T_1:$	$IR \leftarrow M[AR], PC \leftarrow PC + 1$
Decode	$R'T_2:$	$D_0, \dots, D_7 \leftarrow \text{Decode } IR(12-14),$ $AR \leftarrow IR(0-11), I \leftarrow IR(15)$
Indirect	$D_4IT_3:$	$AR \leftarrow M[AR]$
Interrupt:	$T_0T_1T_2(IEN)(FGI + FGO):$	$R \leftarrow 1$ $RT_0:$ $AR \leftarrow 0, TR \leftarrow PC$ $RT_1:$ $M[AR] \leftarrow TR, PC \leftarrow 0$ $RT_2:$ $PC \leftarrow PC + 1, IEN \leftarrow 0, R \leftarrow 0, SC \leftarrow 0$
Memory-reference:		
AND	$D_0T_4:$	$DR \leftarrow M[AR]$
	$D_0T_5:$	$AC \leftarrow AC \wedge DR, SC \leftarrow 0$
ADD	$D_1T_4:$	$DR \leftarrow M[AR]$
	$D_1T_5:$	$AC \leftarrow AC + DR, E \leftarrow C_{out}, SC \leftarrow 0$
LDA	$D_2T_4:$	$DR \leftarrow M[AR]$
	$D_2T_5:$	$AC \leftarrow DR, SC \leftarrow 0$
STA	$D_3T_4:$	$M[AR] \leftarrow AC, SC \leftarrow 0$
BUN	$D_4T_4:$	$PC \leftarrow AR, SC \leftarrow 0$
BSA	$D_5T_4:$	$M[AR] \leftarrow PC, AR \leftarrow AR + 1$
	$D_5T_5:$	$PC \leftarrow AR, SC \leftarrow 0$
ISZ	$D_6T_4:$	$DR \leftarrow M[AR]$
	$D_6T_5:$	$DR \leftarrow DR + 1$
	$D_6T_6:$	$M[AR] \leftarrow DR, \text{ if } (DR = 0) \text{ then } (PC \leftarrow PC + 1), SC \leftarrow 0$
Register-reference:		
	$D_7I'T_3 = r$	(common to all register-reference instructions)
	$IR(i) = B_i$	($i = 0, 1, 2, \dots, 11$)
	$r:$	$SC \leftarrow 0$
CLA	$rB_{11}:$	$AC \leftarrow 0$
CLE	$rB_{10}:$	$E \leftarrow 0$
CMA	$rB_9:$	$AC \leftarrow \overline{AC}$
CME	$rB_8:$	$E \leftarrow \overline{E}$
CIR	$rB_7:$	$AC \leftarrow \text{shr } AC, AC(15) \leftarrow E, E \leftarrow AC(0)$
CIL	$rB_6:$	$AC \leftarrow \text{shl } AC, AC(0) \leftarrow E, E \leftarrow AC(15)$
INC	$rB_5:$	$AC \leftarrow AC + 1$
SPA	$rB_4:$	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	$rB_3:$	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	$rB_2:$	If $(AC = 0)$ then $PC \leftarrow PC + 1$
SZE	$rB_1:$	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	$rB_0:$	$S \leftarrow 0$
Input-output:		
	$D_7IT_3 = p$	(common to all input-output instructions)
	$IR(i) = B_i$	($i = 6, 7, 8, 9, 10, 11$)
	$p:$	$SC \leftarrow 0$
INP	$pB_{11}:$	$AC(0-7) \leftarrow INPR, FGI \leftarrow 0$
OUT	$pB_{10}:$	$OUTR \leftarrow AC(0-7), FGO \leftarrow 0$
SKI	$pB_9:$	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	$pB_8:$	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	$pB_7:$	$IEN \leftarrow 1$
IOF	$pB_6:$	$IEN \leftarrow 0$

