KATHMANDU UNIVERSITY
End Semester Examination [C]
December, 2024

Marks Scored:

Level : B.E./B.Sc.
Year : III

Course : COMP 315
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date 18 DEC 2024

SECTION "A"

[20 Q. × 0.5 = 10 marks]

Choose and mark [X] in the most appropriate option:

1. XOR circuits can be constructed using
   [ ] OR gates only
   [ ] AND, OR gates
   [ ] AND, NOT gates
   [ ] AND, NOT and OR

2. When an inverter is placed between both inputs of an SR flip flop, the resulting flip flop is:
   [ ] JK flip flop
   [ ] D flip flop
   [ ] T flip flop
   [ ] Master slave JK flip flop

3. The m-bit parallel adder consists of
   [ ] (m+1) full adders
   [ ] m/2 full adders
   [ ] m-1 full adders
   [ ] m full adders

4. Which device is used for Parallel to serial conversion of data?
   [ ] Multiplexer [ ] Decoder [ ] Encoder [ ] Register

5. The excess-3 code for 584 is_____
   [ ] 100010110111 [ ] 100001110111 [ ] 100010010110 [ ] 100001010110

6. The decimal number $(-34)_{10}$ is expressed in 2's complement form as
   [ ] 01011110 [ ] 10100010 [ ] 11011110 [ ] 0101110

7. While adding two binary numbers, which gate is used for identifying the overflow condition?
   [ ] XNOR [ ] XOR [ ] OR [ ] NAND

8. What should be the size of multiplexer for constructing a common bus with **k** registers of **n** bits each using multiplexer?
   [ ] k × 1 [ ] (k+1) × 1 [ ] n× 1 [ ] (n+1) × 1

9. Register R contains the binary value 11011101. What will be the sequences of binary values after circular shift-left?
   [ ] 10111010 [ ] 01011101 [ ] 00101110 [ ] 01011100

10. In basic computer instruction formats, if opcode field contains 111, it is_____ instruction.
    a. Memory-reference
    b. Register-reference
    c. Input-output
    [ ] a [ ] b [ ] c [ ] a or b

11. In Branch and save return address (BSA) instruction, the RTL at the execution cycle at T4 is

[ ] D_5T_4: DR←M[AR], AR←AR+1 [ ] D_5T_4: PC←AR, AR←AR+1
[ ] D_5T_4: M[AR]←PC, AR←AR+1 [ ] D_5T_4: M[AR]←AC, AR←AR+1

12. Which of the following characteristics holds TRUE for RISC architecture?
    a) Relatively few instructions
    b) Hardwired Control
    c) Variable length instruction format
    d) Single cycle instruction execution

[ ] a, b & c [ ] b, c & d [ ] a, b & d [ ] a, c & d

13. Consider the two 8-bit numbers A=01000001 and B= 10000100. Add the two binary numbers assuming that the numbers are represented in 2's complement form. After performing **add** operation which conditional branch instruction will have true condition?

[ ] Branch if Zero [ ] Branch if overflow
[ ] Branch if minus [ ] Branch if carry

14. Which of the following addressing modes uses a pointer to access memory indirectly?

[ ] Immediate Addressing Mode [ ] Register Indirect Addressing Mode
[ ] Direct Addressing Mode [ ] Relative Addressing Mode

15. In an unsigned multiplication algorithm, if the least significant bit of multiplier is 0, then what operation will you perform?

[ ] Addition [ ] Subtraction
[ ] Arithmetic shift right [ ] Logical shift right

16. In binary division the sign of the remainder is same as the sign of _____

[ ] quotient [ ] dividend
[ ] divisor [ ] sequence counter

17. The CPU nearly delays its operation for one memory cycle, to allow direct memory I/O transfer. This process is called

[ ] Burst transfer [ ] Cycle waiting
[ ] Cycle stealing [ ] Cycle interrupting

18. In daisy chaining method device with PI=____ and PO=____ is the one with higher priority that is requesting an interrupt

[ ] 1, 0 [ ] 0, 1 [ ] 1, 1 [ ] 0, 0

19. What is/are true regarding Set Associative Mapping in cache memory organization?
    a. Improve hit ratio
    b. Table sizes vary based upon number of data to be accommodated
    c. Replacement algorithm cannot be used

[ ] a & c [ ] a only [ ] a & b & c [ ] a & b

20. What is the typical characteristic of memory as you move down the memory hierarchy from registers to secondary storage?

[ ] Increased speed and cost [ ] Decreased speed and increased cost
[ ] Decreased speed and cost [ ] Increased speed and decreased cost

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SECTION "B"

[6 Q. × 4 = 24 marks]

Attempt ANY SIX questions.

1. Describe the Von Neumann's envisioned structure of a Computer System? Describe how read and write operations are performed in Random Access Memory with suitable block diagram? [2+2]

2. What is the drawback with BCD? How it can be overcome by certain weighted code, describe it with example? Perform the arithmetic operation $(-52)_{10} + (-5)_{10}$ using signed-2's complement representation? [2+2]

3. A 6-bit register contains the binary value 110010. What is the register value after arithmetic shift right? Draw the block diagram and describe the operation for the hardware that implements the following statements:

   $x + yz$: **AR ←AR + BR**

   Where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function. [1+3]

4. As a computer designer, when will you say that an instruction set of a computer is complete? Design a common bus for a basic computer with single accumulator organization, which has 8 registers [DR(16 bit), AR(12 bit), AC(18bit), IR(18 bit), PC(12 bit), TR(18 bit), INPR(8 bit), OUTR(8 bit)], a memory unit(4096×16) and Adder and logic unit with overflow flag(E), this ALU has 3 sets of input (AC, DR and INPR) and output to AC? Explain why the given microoperation **(IR←M[PC])** cannot execute during the single clock pulse in the system with above common bus configuration. Specify the sequence of microperations that will perform the operation [1+2+1]

5. The given expression is needed to be converted into program. Write three address, two address, one address and zero address instruction for the given expression. [1+1+1+1]

   X= (A * B – C + D / E) * G / H

6. Discuss interrupt handling method for Parallel Priority Interrupt. [4]

7. Differentiate between write through and write back procedures for writing into cache? Describe Direct mapping organization of Cache Memory [1+3]

SECTION "C"

[2 Q. × 8 = 16 marks]

Attempt ANY TWO questions.

8. Explain with flowchart for adding and subtracting two fixed-point binary numbers using signed magnitude representation? Show the step-by-step division process using Booth's algorithm for performing $(-17)_{10} \times (-5)_{10}$. [4+4]

9. What are the fundamental differences between strobe pulse method and handshaking method? With necessary figures and RTL, discuss the Fetch, Decode, indirect and Execute cycle of ADD and ISZ. [3+5]