KATHMANDU UNIVERSITY
End Semester Examination
August, 2018

AUG 16 2018

Level : B. Sc.
Year : III

Course : COMP 315
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date :

SECTION "A"
[20 Q × 0.5 = 10 marks]

Tick (√) the correct answer(s).

1. The binary code equivalent of $(1100110)_{gray}$ is
[ ] 1100010 [ ] 1000110 [ ] 1000111 [ ] 1000100

2. Which technique is used that identifies the highest priority resource by means of software:
[ ] Daisy chaining [ ] Polling [ ] Priority [ ] Chaining

3. In memory-mapped scheme, the devices are viewed as
[ ] distinct I/O devices [ ] memory locations
[ ] only input devices [ ] only output devices

4. Micro-operations are loosely categorized in..... types.
[ ] 2 [ ] 3 [ ] 4 [ ] 5

5. DMA is particularly suited for data transfer between the _____.
[ ] Disk drive and CPU [ ] Disk drive and RAM
[ ] Disk drive and ROM [ ] Disk drive and I/O

6. A stack pointer is
[ ] A register in the processor that indicates the beginning of stack memory
[ ] A register that decodes and execute arithmetic instruction
[ ] A first memory location where a subroutine address is stored
[ ] A register in which a flag is stored

7. Which operations are implemented using a binary counter or a combinational circuit?
[ ] Shifting [ ] logical [ ] transfer [ ] arithmetic

8. In Register transfer language which one is explicit representation
[ ] BUS ← R1, R2 ←BUS [ ] R1 ← R2
[ ] R2 ← R1 [ ] R1 ← BUS, R3 ← BUS

9. The m-bit parallel adder consists of
[ ] (m+1) full adders [ ] m/2 full adders
[ ] m-1 full adders [ ] m full adders

10. The Excess-3 decimal code is a self-complementing code because
(I) The binary sum of a code and its 9's complement is equal to 9.
(II) The binary sum of a code and its 10's complement is equal to 9.
(III) Complement can be generated by inverting each bit pattern.
[ ] I only [ ] I and II only [ ] I and III only [ ] II and III only

11. In ISZ instruction, the RTL at the execution cycle T_5 is

[ ] D_6T_5: DR←DR+1 [ ] D_6T_5: DR ← M [AR]

[ ] D_6T_5: M [AR] ← DR [ ] D_6T_5: DR ← DR +1, SC ← 0

12. To execute the RTL statement **M[AR] ← IR,** Which line of IR should go high?

[ ] Clear [ ] Increment [ ] Load [ ] Clock

13. How can you decrement a value stored in 8 bit register

[ ] By adding 8 1's in the original value

[ ] By subtracting 8 1's in the original value

[ ] First add 8 1's in the original value then subtract

[ ] Decrement operation cannot be implemented

14. To fetch an instruction from memory to instruction cycle, we need

[ ] T_0 cycle [ ] T_0 and T_1 cycle

[ ] T_0, T_1 and T_2 cycle [ ] T_1 and T_2 cycle

15. Which is **not an** equivalent representation of $(-25)_{10}$ in 2's complement form.

[ ] 100111 [ ] 11100111 [ ] 111100111 [ ] 111110111

16. Consider the following logic function f (ABC).

F (A, B, C) = (A + B + C'). (A + B'+ C')

Which of the following would be the result if the above logic function is to be simplified using k-maps?

[ ] C' + A [ ] C + C'A' [ ] C'.A [ ] C'.A' + B

17. The _____ operation sets to 1 the bits in one register where there are corresponding 1's in the second register.

[ ] Selective Complement [ ] Selective Clear

[ ] Selective Set [ ] Insert

18. If F= AB' + C'D then F'= ------

[ ] (A+B') (C'+D) [ ] (A'B) + (CD') [ ] (AB') (CD') [ ] (A'+B) (C+D')

19. In a 3-bit parity system, the parity output from parity generator is 1 and output from parity checker is 1, which of the following is true

[ ] System is using odd parity and transfer has some problem

[ ] System is using odd parity and transfer has no problem

[ ] System is using even parity and transfer has some problem

[ ] System is using even parity and transfer has no problem

20. Which one best describes ASHR operation?

[ ] 2's complement and divide by 2 and ceiling

[ ] 2's complement and multiply by 2 and floor

[ ] 2's complement and multiply by 2 and ceiling

[ ] 2's complement and divide by 2 and floor

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SECTION "B"
[6Q × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. Briefly discuss addition rules for signed magnitude, signed 1's complement and signed 2's complement numbers.

2. Discuss the working principle of an arithmetic circuit that can perform 8 basic operations. The operations are add, add with carry, subtract with borrow, subtract, transfer, increment and decrement. Illustrate it with a diagram.

3. Branch unconditionally is an instruction used by CPU to skip certain portion of a program and jump to a label defined by user. Discuss how it is done with reference to fetch, decode and execution cycle.

4. Draw memory stack organization and briefly explain zero address instruction. [3+1]

5. Draw the block diagram for signed magnitude multiplication and Booth's algorithm. [2+2]

6. With neat diagram, discuss the working principle of 3 * 4 FIFO BUFFER.

7. With a diagram, discuss DMA transfer. Elaborate you answer for DMA as an I/O, as an input and as an output.

SECTION "C"
[2Q × 2 =16 marks]

Attempt *ANY TWO* questions.

8. In order to perform division between two values, first you need to check for an overflow. Illustrate, how this is done in division algorithm for signed magnitude numbers? Divide (-55) by (+7). Assume that the values are signed magnitude numbers. Draw flowchart of addition and subtraction algorithm for signed magnitude representation. [2+3+3]

9. Illustrate the use of ASHR and ASHL operations with an example of your choice. Briefly discuss the application of logical micro-operations. Draw a block diagram of ALU that can perform arithmetic, logical and shifting micro-operations. [3+3+2]

10. COMPARE is an instruction use to compare two values. Illustrate with an example, how you can compare two unsigned numbers. Illustrate the decode cycle and execution cycle of RRI instruction. Assume CLA is an instruction for this purpose. Write down the RTL of interrupt cycle. [3+3+2]