Mark Scored:

KATHMANDU UNIVERSITY
End Semester Examination
August/September, 2017

Level : B. Sc.
Year : III
Course : COMP 315
Semester : I

Exam Roll No. :
Time: 30 min
F. M. : 10

Registration No.:
Date SEP 04 2017

SECTION "A"
[20 Q × 0.5 = 10 marks]

Tick (√) the correct answer(s).

1. What is the 2's complement representation of -24 in a 16 bit bit micro-computer?
[ ] 0000 0000 0001 1000
[ ] 1111 1111 1110 0111
[ ] 1111 1111 1110 1000
[ ] 1111 1111 1101 1000

2. A hand-shake based protocol for data transfer is an example of _____ type of data transfer.
[ ] Synchronous [ ] Asynchronous [ ] Serial [ ] Indirect

3. In daisy chaining method device with PI=____and PO=____is the one with higher priority that is requesting an interrupt.
[ ] 1, 0 [ ] 0, 1 [ ] 1, 1 [ ] 0, 0

4. The Excess-3 decimal code is a self-complementing code because
(I) The binary sum of a code and its 9's complement is equal to 9.
(II) The binary sum of a code and its 10's complement is equal to 9.\
(III) Complement can be generated by inverting each bit pattern.
[ ] I only [ ] I and II only [ ] I and III only [ ] II and III only

5. The largest integer that can be represented in 2's complement number using n bits is _
[ ] 2^n-1 [ ] 2^n [ ] 2^{n-1} -1 [ ] 2^{n-1}

6. The least negative value that the product of two 8 bits 2's complement number can take is _____
[ ] -2^{14} [ ] -2^{15} [ ] -2^{10} [ ] -2^{12}

7. Which shift is a shift micro operation which is used to shift a signed binary number to the left or right_____
[ ] Logical [ ] Arithmetic [ ] Circular [ ] rotate

8. In a vectored interrupt_____
[ ] the branch address is assigned to a fixed location in memory.
[ ] the interrupting source supplies the branch information to the processor through an interrupt vector.
[ ] the branch address is obtained from a register in the processor
[ ] the branch address is not available

9. A stack organized computer use _____ addressing
[ ] Indexed [ ] one [ ] Two [ ] zero

10. If the value of the target operand is contained in the address field itself, the addressing mode is:
[ ] immediate [ ] direct [ ] indirect [ ] implied

11. What is the content of Stack Pointer (SP)?
[ ] Address of the current instruction [ ] Address of the next instruction
[ ] Address of the top element of the stack [ ] Size of the stack

12. In daisy chaining method of interrupt handing, devices are connected in_____ manner.
[ ] Parallel [ ] Random [ ] Serial [ ] Synchronous

13. What is the operation that sets to 1 the bits in one register where there is corresponding 1's in the second register?
[ ] Selective clear [ ] Selective set
[ ] Selective Complement [ ] Insert

14. Which of the following describes the Mnemonic SPA?
[ ] Skip If (Address Resister) Positive [ ] Skip If (Accumulator) Positive
[ ] Skip If (Adder-Subtractor) Positive [ ] Skip If (Associative Mapping) Positive

15. To execute the RTL statement **$R'T_0$: AR←PC,** Which line of PC should go high?
[ ] Clear [ ] Increment [ ] Load [ ] Clock

16. In binary division the sign of the remainder is same as the sign of _____
[ ] quotient [ ] dividend [ ] divisor [ ] sequence counter

17. Register R contains the binary value 10011100. What will be the sequences of binary values after arithmetic shift right?
[ ] 01001110 [ ] 11001110 [ ] 00111000 [ ] 00111001

18. What does the m-bit parallel adder consists of?
[ ] (m+1) full adders [ ] m/2 full adders
[ ] m-1 full adders [ ] m full adders

19. The register that keeps track of the instructions in the program stored in memory is __
[ ] Accumulator [ ] Program counter
[ ] temporary register [ ] Instruction register

20. The device which is used to connect a peripheral to bus is called _____
[ ] Control register [ ] Interface
[ ] Communication protocol [ ] decoder

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SECTION "B"

[6Q × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. Discuss the use of logical micro-operation. Compare among logical, circular and arithmetic shift. [1+3]

2. Briefly explain relative addressing modes with necessary types.

3. What is Interrupt cycle of a basic computer? Explain with flow chart.

4. Discuss the working principle of a FIFO buffer.

5. Using Booth's Algorithm, perform $(-11)_{10} \times (+10)_{10}$?

6. Represent the given expression using three addresses, two addresses, one address and zero address formats.
   X= (A + B * C / D + F – G)

7. Explain General Register Organization and Stack Organization of CPU. [4]

SECTION "C"

[8Q × 2 =16 marks]

Attempt *ANY TWO* questions.

8. Discuss parity generator and parity checker. Design the load, increment and clear signal of an accumulator as well as the ALU based upon the table given below. [3+2+3]

9. Draw flowchart for adding and subtracting two fixed-point binary numbers using signed magnitude representation. Test algorithm when values in addend and augend are -5 and +7 respectively and the operator is addition. Divide (-21) by (+4). [5+3]

10. Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2, 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, 7, the binary output is one less than the input. Design an arithmetic circuit with one selection variable S and two n–bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram of first 2 MSB's. [4+4]

S	$C_{in} = 0$	$C_{in} = 1$
1	D= A – 1 (Decrement)	D = A+ B' + 1 (Subtract)
0	D = A+B (Add)	D = A+ 1 (Increment)

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$,
		$AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	D_7IT_3:	$AR \leftarrow M[AR]$
Interrupt:		
	$T_0'T_1'T_2'(IEN)(FGI + FGO)$:	$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$
Register-reference:		
		$D_7I'T_3 = r$ (common to all register-reference instructions)
		$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$
	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow$ shr AC, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow$ shl AC, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1)$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$
Input-output:		
		$D_7IT_3 = p$ (common to all input–output instructions)
		$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$
	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$