

KATHMANDU UNIVERSITY
End Semester Examination [C]
April/May, 2023

Marks Scored:

Level : B.E./B.Sc.
Year : III

Course : COMP 315
Semester : I

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date 28 APR 2023

SECTION "A"

[20Q. × 0.5 = 10 marks]

Mark [×] for the most appropriate alternative or fill in the blanks.

- On a Karnaugh map, grouping the 0s produces
 a product-of-sums expression a "don't care condition"
 a sum-of-products expression AND-OR logic
- When an inverter is placed between both inputs of an SR flip flop, the resulting flip flop is:
 JK flip flop D flip flop
 T flip flop Master slave JK flip flop
- The m-bit parallel adder consists of
 (m+1) full adders m/2 full adders
 m-1 full adders m full adders
- In 4 bit binary counter with parallel load and synchronous clear, when clock pulses are applied to the Clock terminal, Clear input is 0, Load and Increment input is 1, what operation will it perform?
 No change Increment Counter by 1
 Load inputs Clear outputs to 0
- What is the binary code for a decimal digit 6 in Excess-3 code?
 0110 1100 1001 1101
- The decimal number (-34)₁₀ is expressed in 2's complement form as
 01011110 10100010 11011110 01011110
- The representation of (-17)₁₀ in ANSI 32-bit floating point numbers in byte format is
 00000101 10001000 00000000 00000000
 10000100 01000100 00000000 00000000
 10001011 10001000 00000000 00000000
 10000101 10001000 00000000 00000000
- How many decoders are required to construct a common bus for k registers of n bits each using 3-state buffers?
 k k+1 n n+1
- Which operation sets to 1 the bits in register A where there is corresponding 1's in the register B?
 Selective clear Selective set
 Selective Complement Insert

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SECTION "B"
[6Q. × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. Differentiate between computer organization and computer architecture? Describe about two different types of ROMs? [2+2]
2. What are the advantage of Signed 2's complement representation over Signed magnitude representation and Signed 1's complement representation? Derive the circuits for a 3-bit parity generator and 4-bit parity checker using an even-parity bit? [1+3]
3. Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in} . Draw the logic diagram of first 2 MSB's.

S	$C_{in}=0$	$C_{in}=1$
1	$D = A - 1$ (Decrement)	$D = A + B' + 1$ (Subtract)
0	$D = A + B$ (Add)	$D = A + 1$ (Increment)

4. Describe the complete instruction cycle for the basic computer while executing an instruction *ISZ (Increment and Skip if zero)* with a suitable flowchart?
5. Describe two different types of CPU organization? A two-word instruction is stored in memory at an address designated by the symbol **W**. The address field of an instruction (stored at **W+1**) is designated by the symbol **Y**. The operand used during the execution of the instruction is stored at an address symbolized by **Z**. An index register contains the value **X**. State how **Z** is calculated from the other addresses if the addressing mode of the instruction is a) Immediate b) Indirect c) Relative d) Indexed [2+2]
6. Explain the priority interrupt handling using daisy chaining.
7. A digital computer has a memory unit of $64K \times 16$ and cache memory of 1K words. The cache uses direct mapping with a block size of four words.
 - a. How many bits are there in the tag, index, block, and word fields of the address format?
 - b. How many words are bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
 - c. How many blocks can the cache accommodate?

SECTION "C"
[2Q. × 8 = 16 marks]

Attempt *ALL* questions.

8. Explain with flowchart for adding and subtracting two fixed-point binary numbers using signed magnitude representation? Show the step-by-step division process using 2's complement division algorithm for performing $(-17)_{10} / (-5)_{10}$. [4+4]
9. What are the fundamental differences between strobe pulse method and handshaking method? With necessary figures and RTL, discuss the Fetch, Decode and Execute cycle of ADD and ISZ. [3+5]

