KATHMANDU UNIVERSITY
End Semester Examination
May/June, 2022

Marks Scored:

Level : B.E./B.Sc.
Year : II

Course : COMP 231
Semester : II

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date :

SECTION "A"
[20Q. × 0.5 = 10 marks]

Tick [√] the most appropriate answer from the alternatives given. All symbols have their usual meanings.

1. In 8085, which are 16 bit registers?
   [ ] Stack counter and accumulator
   [ ] Program Counter and Accumulator
   [ ] Stack Pointer and Program Counter
   [ ] Accumulator, Stack Pointer and Program Counter

2. The instruction, MOV AX, 1234H is an example of
   [ ] Register addressing mode [ ] Immediate addressing mode
   [ ] Based indexed addressing mode [ ] Direct addressing mode

3. If the programmable counter timer 8254 is set in mode 1 and is to be used to count six events, the output will remain at logic 0 for _____ number of counts.
   [ ] 4 [ ] 5 [ ] 6 [ ] 7

4. The _____ can refer to either the time period during which one instruction is fetched from memory and executed when a computer receives a machine language instruction.
   [ ] Instruction cycle [ ] Instruction fetch operation
   [ ] Memory data register [ ] Instruction decoder

5. _____ is used to accept data from outside devices to store in the accumulator.
   [ ] Immediate addressing [ ] Direct addressing
   [ ] Register addressing [ ] Indirect addressing

6. In which T-state does the CPU sends the address to memory or I/O and the ALE signal for demultiplexing?
   [ ] T1 [ ] T2 [ ] T3 [ ] T4

7. Number of the times the instruction sequence below will loop before coming out of loop is MOV AL, 00H A1: INC AL JNZ A1 is
   [ ] 0 [ ] 1 [ ] 255 [ ] 256

8. _____ occurs during the first clock cycle of a machine state and enables the address to get latched into the on chip latch of peripherals.
   [ ] ALE [ ] HOLD [ ] READY [ ] INTR

9. The _____ ensures that only one IC is active at a time to avoid a bus conflict caused by two ICs writing different data to the same bus
[ ] Control bus [ ] control instructions
[ ] Address decoder [ ] CPU

10. The result of MOV AL, 65 is to store
[ ] 0100 0010 in AL [ ] 42H in AL
[ ] 40H in AL [ ] 0100 0001 in AL

11. Which method dose bypass the CPU for certain types of data transfer?
[ ] Direct memory access [ ] Software interrupts
[ ] Interrupt-driven I/O [ ] Polled I/O

12. In 8086 microprocessor which of the following statements is **NOT TRUE**?
[ ] Coprocessor is interfaced in max mode [ ] It supports pipelining
[ ] Coprocessor is interfaced in min mode [ ] I/O can be interfaced in max / min mode

13. Which statement is **TRUE** for DMA?
[ ] It allows certain hardware subsystems to read/write data to/from memory
[ ] 64 KByte section of memory address capability with multiple programming
[ ] Software instruction has different effect as the hardware reset
[ ] DMA channel can be programmed to manually set up and start another DMA transfer

14. _____ signal prevent the microprocessor from reading the same data more than one
[ ] Pipelining [ ] Handshaking [ ] Controlling [ ] Signaling

15. The _____ of the memory chip will identify and select the register for the EPROM
[ ] Internal decoder [ ] External decoder
[ ] Address decoder [ ] Data decoder

16. In the operand fetch stage, the floating point unit fetches the operands from
[ ] Floating point unit [ ] Instruction cache
[ ] Floating point register file [ ] Low power consumption

17. _____ tells the I/O device to release its data into the data bus.
[ ] IORC [ ] MWTC [ ] AMWC [ ] AIOWC

18. When non-specific EOI command is issued to 8259A it will automatically
[ ] Set the ISR [ ] Reset the ISR [ ] Set the INTR [ ] Reset the INTR

19. Which statement is valid for LDA 9511H?
[ ] Store the result from A to 9511
[ ] Load the contents of 9511 in register A
[ ] Transfer the contents of A to B register
[ ] Move the results from 9511 to A

20. Which of the following command is used to make all the internal registers of 8237 clear?
[ ] Clear first/last flip flop [ ] Clear priority register
[ ] Clear mask register [ ] Master clear command

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SECTION "B"
[6Q. × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. Discuss X86 Registers. What are the memory addressing modes of X86 Microprocessor?

2. Mention data transfer mechanism using DMA Controller. What are DMA transfer modes?

3. Explain machine cycle and its categories. Define interfacing memory and I/O ports of 8086 Microprocessor.

4. What are the control and status signals of 8085 Microprocessor? Describe Instruction Set classification of Intel 8085.

5. Differentiate between subroutine and trap. Discuss parameter passing in registers and transparent subroutine with an example.

6. Explain pin diagram of Intel 8259. What are the Registers found in 8259?

7. Mention 8086 addressing modes with example.

SECTION "C"
[2Q. × 8 = 16 marks]

Attempt *ANY TWO* questions.

8. Explain Control Buses in 8288 along with functional block diagram. Briefly mention the transfer modes of DMA.

9. Discuss internal architecture of 8086 Microprocessor with a figure. Mention the Assemble Directives available in 8086.

10. What are the features and applications of 8254 programmable interval timer? Explain its operating modes with wave forms.