KATHMANDU UNIVERSITY
End Semester Examination
June/July, 2023

Marks Scored:

Level : B.E./B.Sc.
Year : II
Course : COMP 231
Semester : II
Exam Roll No. :
Time: 30 mins.
F. M. : 10
Registration No.:
Date 06 JUL 2023

SECTION "A"
[20 Q. × 0.5 = 10 marks]

Mark **[X]** in the most appropriate option. All symbols have their usual meanings.

1. _____ is used as a special signal to demultiplex the address bus and data bus.
   [ ] Priority Encoder [ ] Address Latch Enable
   [ ] Demultiplexer [ ] Decoder

2. Which components are **NOT** found on chip in a microprocessor but may be found on chip in a microcontroller?
   [ ] SRAM & USART [ ] EPROM & PORTS
   [ ] EPROM, USART & PORTS [ ] SRAM, EPROM & PORTS

3. One of the main feature that distinguish microprocessors from microcomputers is
   [ ] Words are usually larger in microprocessors
   [ ] Words are shorter on microprocessors
   [ ] Microprocessor does not contain I/O devices
   [ ] Exactly the same as the machine cycle time

4. The result of MOV AL, 65 is to store
   [ ] Store 0100 0010 in AL [ ] Store 40H in AL
   [ ] Store 42H in AL [ ] Store 0100 0001 in AL

5. The length of bus cycle in 8086/8088 is four clock cycles, T_1, T_2, T_3, T_4 and an indeterminate number of wait state clock cycles denoted by T_w. The wait states are always inserted between
   [ ] T_1 & T_2 [ ] T_2 & T_3 [ ] T_3 & T_4 [ ] T_4 & T_1

6. When non-specific EOI command is issued to 8259A it will automatically
   [ ] Set the ISR [ ] Reset the ISR [ ] Set the INTR [ ] Reset the INTR

7. The DMA controller uses _____ to help with the transfers when handling network interfaces.
   [ ] Input Buffer storage [ ] Signal enhancers
   [ ] Bridge circuits [ ] Memory con

8. Consider the following set of 8085 instruction.

```
        MVI A,82H
        ORA A
        JP DSPLY
        XRA A
DSPLY:OUT PORT1
        HLT
```

   The output at PORT1 is
   [ ] 00H [ ] FFH [ ] 92H [ ] 11H

9. The block of 8237 that decodes the various commands given to the 8237 by the CPU is
[ ] Timing and control block [ ] Program command control block
[ ] Priority block [ ] Current address register block

10. Which statement is **TRUE** for DMA?
[ ] DMA channel can be programmed to manually set up and start another DMA transfer
[ ] It allows certain hardware subsystems to read/write data to/from memory
[ ] 64 KByte section of memory address capability with multiple programming
[ ] Software instruction has different effect as the hardware reset

11. Intel 8088 CPU has both BIU and EU. Which one of these statements is **CORRECT**?
[ ] Both of them works to calculate address
[ ] ALU in BIU counts data
[ ] EU is used for data calculation instead of address
[ ] BIU is a Base Instruction Unit

12. If the instruction is MOV AL, [1000] with DS=0100H, which one is the physical address which data will be written into AL?
[ ] 02000H [ ] 11000H [ ] 1100H [ ] 0200H

13. In 8085 microprocessor system with memory mapped I/O, which of the following is **TRUE**?
[ ] Devices have 8-bit address line
[ ] Devices are accessed using IN and OUT instructions
[ ] There can be maximum of 256 input devices and 256 output devices
[ ] Arithmetic and logic operations can be directly performed with the I/O data

14. Which of the following is **NOT** a property of TRAP interrupt in microprocessor?
[ ] It uses edge-triggered signal [ ] It is a vectored interrupt
[ ] It is a non-maskable interrupt [ ] It is of highest priority

15. In mode 2 of Programmable Interval Timer 8254, if N is loaded as the count value, then after (N-1) cycles, the output becomes low for
[ ] 1 clockcycle [ ] 2 clockcycles [ ] 3 clockcycles [ ] 4 clockcycles

16. MOV AX, [1234H] Type of addressing mode used for
[ ] Immediate addressing mode [ ] Direct addressing mode
[ ] Register relative mode [ ] Base index mode

17. In Maximum Mode of 8086 Microprocessor control bus signal S0, S1 and S2 are sent out in _____form
[ ] Decoded [ ] Encoded [ ] Shared [ ] Unshared

18. Which of the following is the **CORRECT** sequence of operations in a microprocessor?
[ ] Opcode fetch, memory read, memory write, I/O read, I/O write
[ ] Opcode fetch, memory write, memory read, I/O read, I/O write
[ ] I/O read, opcode fetch, memory read, memory write, I/O write
[ ] I/O read, opcode fetch, memory write, memory read, I/O write

19. A memory connected to a microprocessor has 20 address lines and 16 data lines. What will be the memory capacity?
[ ] 8 KB [ ] 2 MB [ ] 16 MB [ ] 64 KB

20. In 8086 the overflow flag is set when
[ ] The sum is more than 16 bits
[ ] Subtraction
[ ] Carry and sign flags are set
[ ] Signed numbers go out of their range after an arithmetic operation

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SECTION "B"
[6Q. × 4= 24 marks]

Attempt *ANY SIX* questions.

1. What is the function of program counter in microprocessor? Explain briefly what happens when the INTR signal goes High in 8085?

2. Mention the complete bit configuration of 8085 flag register. Explain the Software and Hardware interrupts of 8085.

3. What are the different types of instructions in 8086 microprocessor? Write a program to add a data byte located at offset 0400H in 3000H segment to another data byte available at 0500H in the same segment and store the result at 0800H in the same segment.

4. What is design interfacing of 8282 latches to 8086 system? Explain bus transceiver 8286 with diagram.

5. Describe internal block diagram of 8259 programmable interval timer.

6. Explain the use of 8288 bus controller and in which mode it is used. Illustrate with a block diagram, major parts of 8288 controllers.

7. How does a stack work in assembly language? What are the conditional CALL statements in assembly language?

SECTION "C"
[2Q. × 8 = 16 marks]

Attempt *ANY TWO* marks.

8. a. What are the conditional CALL statements in assembly language?

   b. What do you mean by addressing mode? Explain all the addressing mode available in 8086 microprocessor with an example.

9. Explain the modes of operation in 8254 programmable Interval timer. Mention the features of 8254 microprocessor with its pin diagram.

10. Define Direct Memory Access (DMA). Explain about DMA controller 8237 interfacing with microprocessor and explain its operation process in details.