

KATHMANDU UNIVERSITY  
End Semester Examination [C]  
January, 2018

Marks Scored:

Level : B.E./B.Sc.  
Year : II

Course : COMP 231  
Semester: II

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date JAN 11 2018

SECTION "A"

[20 Q.×0.5=10 marks]

Tick [√] the most appropriate answer from the alternatives given. All symbols have their usual meanings.

- After every response to the single step interrupt the flag that is cleared is \_\_\_\_\_.  
 IF (Interrupt Flag)                       TF (Trap Flag)  
 OF (Overflow Flag)                       IC (Interrupt Controller)
- If 'n' denotes number of clock cycles and 'T' denotes period of the clock at which the microprocessor is running, then duration of execution of loop once can be denoted by  
 n+T                       n-T                       n\*T                       n/T
- In an 8085 microprocessor, the instruction CMP B has been executed while the content of accumulator is less than that of register B. As a result carry flag and zero flag will be \_\_\_\_\_.  
 Set, reset                       Reset, set                       Reset, reset                       Set, set
- The number of instructions actually executed by the microprocessor depends on the  
 Stack                       Loop count                       program counter                       Time duration
- When large delays are required, then to serve the purpose  
 One or more count registers can be used  
 One or more shift registers can be used  
 One or more pointer registers can be used  
 One or more index registers can be used
- To put the 8085 microprocessor in the wait state  
 Lower the-HOLD input                       Lower the READY input  
 Raise the HOLD input                       Raise the READY input
- Interfacing devices for DMA controller, programmable interval timer are respectively  
 8257, 8253                       8253, 8257                       8257, 8251                       8251, 8257
- In the instruction set:  
MOV CX, BA03H  
WAIT: DEC CX  
NOP  
JNZ WAIT  
RET  
if the zeroth condition is satisfied then, for execution, the JNZ instruction takes  
 1 clock cycle                       2 clock cycle                       3 clock cycle                       4 clock cycle

9. In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is \_\_\_\_\_.
- Non-maskable and non-vectorized       Maskable and non-vectorized  
 Non-maskable and vectored       Maskable and vectored
10. The necessary steps carried out to perform the operation of accessing either memory or I/O Device, constitute a \_\_\_\_\_.
- Fetch operation       Execute operation  
 Machine cycle       instruction cycle
11. The number of Interrupt lines in 8085 is \_\_\_\_\_.
- 2       3       4       5
12. An input output processor controls the flow of information between
- Cache memory and I/O devices       Main memory and I/O devices  
 Two I/O devices       Cache and main memory
13. DB, DW and DD directives are used to place data in particular location or to simply allocate space without preassigning anything to space. The DW and DD directories are used to generate:
- Offsets  
 Full address of variables  
 Full address of labels  
 Offsets of full address of labels and variables
14. The operation, IOWR (active low) performs
- Write operation on input data       Write operation on output data  
 Read operation on input data       Read operation on output data
15. Which of the following command is used to make all the internal registers of 8237 clear?
- Clear first/last flipflop       Master clear command  
 Clear mask register       Demand transfer command
16. Which statement is valid for LDA 9617H?
- Input port is loaded into input latches       Input port is loaded into output latches  
 Output port is loaded into input latches       Output port is loaded into output latches
17. The transfer of a block of data from one set of memory address to another takes place in
- Block transfer mode       Demand transfer mode  
 Memory to memory transfer mode       Cascade mode
18. The DMA request input pin that has the highest priority is \_\_\_\_\_.
- DREQ0       DREQ1       DREQ2       DREQ3
19. \_\_\_\_\_ generates interrupt signal to microprocessor and receives acknowledge.
- Priority resolver       Control logic  
 Interrupt request register       Interrupt register
20. The register that keeps track of all the DMA channel pending requests, and status of their terminal counts is \_\_\_\_\_.
- Mask register       Request register       Status register       Count register

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SECTION "B"

[6 Q.×4=24 marks]

Attempt *ANY SIX* questions.

1. What is Microprocessor? Mention features of Analytical Engine.
2. Define Assembly Language. Describe history of Microprocessor.
3. Mention control and status signals of Intel 8085. Briefly describe addressing modes of 8086 microprocessor.
4. What do you mean by Basic State Transitions? Explain bus transceiver 8286 with diagram.
5. Define Instruction Queue and Instruction Pointer. Describe pin diagram of 8254 programmable interval timer.
6. Differentiate between 8086 and 8088 Microprocessors.
7. What is subroutine? Describe memory organization in 8086.

SECTION "C"

[2 Q.×8=16 marks]

Attempt *ANY TWO* questions.

8. What is machine cycle? Explain 8086 CPU registers.
9. What is Interrupt? Explain functional block diagram of 8259A.
10. Describe DMA transfer modes. Explain pin diagram of 8237.

