KATHMANDU UNIVERSITY
End Semester Examination
January/February 2024

Marks Scored:

Level : B.E./B.Sc.
Year : II

01 FEB 2024

Course : COMP 231
Semester : II

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date :

SECTION "A"

[20Q. × 0.5 = 10 marks]

Choose and mark [X] in the most appropriate option from each set of choices

1. In 8237, if each device connected to a channel is assigned to a fixed priority then it is said to be in _____.
   [ ] Rotating priority scheme
   [ ] Fixed priority scheme
   [ ] Rotating priority and fixed priority scheme
   [ ] Interrupt stage

2. The TRAP is one of the interrupts available its INTEL 8085. Which one of the following statements is true of TRAP?
   [ ] It is level triggered
   [ ] It is positive edge triggered
   [ ] It is negative edge triggered
   [ ] It is both positive edge triggered and level triggered

3. In the instruction set,

```
MOV CX, BA03H
WAIT: DEC CX
NOP
JNZ WAIT
RET
```

   if the zeroth condition is satisfied then, for execution, the JNZ instruction takes
   [ ] 1 clock cycle [ ] 2 clock cycles [ ] 3 clock cycles [ ] 4 clock cycles

4. The _____ can refer to either the time period during which one instruction is fetched from memory and executed when a computer receives a machine language instruction.
   [ ] Instruction fetch operation
   [ ] Instruction cycle
   [ ] Memory data register
   [ ] Instruction decoder

5. DB, DW and DD directives are used to place data in particular location or to simply allocate space without pre-assigning anything to space. The DW and DD directories are used to generate:
   [ ] Offsets
   [ ] Full address of variables
   [ ] Full address of labels
   [ ] Offsets of full address of labels and variables

6. In the instruction set,

```
MOV CX, BA03H
WAIT: DEC CX
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JNZ WAIT
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```

if the zeroth condition is satisfied then, for execution, the JNZ instruction takes
[ ] 1 clock cycle [ ] 2 clock cycles [ ] 3 clock cycles [ ] 4 clock cycles

7. What type of control pins are needed in a microprocessor to regulate traffic on the bus in order to prevent two devices from trying to use it at the same time?
[ ] Bus arbitration [ ] Interrupts [ ] Bus control [ ] Status

8. In control word format, if RL1=1, RL0=1 then the operation performed is
[ ] Read/load least significant byte only [ ] Read/load most significant byte only
[ ] Read/load LSB first and then MSB [ ] Read/load MSB first and then LSB

9. To indicate the I/O device that its request for the DMA transfer has been honored by the CPU, the DMA controller pulls
[ ] HLDA signal [ ] HRQ signal
[ ] DACK (active low) [ ] DACK (active high)

10. While using a frequency counter for measuring frequency, two modes of measurement are possible: Period time and Frequency mode. There is a 'cross-over frequency' below which the period mode is preferred. Assuming the crystal oscillator frequency to be 4MHz, the crossover frequency is given by
[ ] 8 MHz [ ] 2 MHz [ ] 5 KHz [ ] 1 KHz

11. If the contents of SP are 1000H, PUSH B instruction will transfer the contents of registers B & C respectively for memory locations
[ ] 0FFF H and 0FFE H [ ] 0FFE H and 0FFF H
[ ] 1000 H and 0FFF H [ ] 1000 H and 1001 H

12. BHE pin of 8086 Microprocessor signal is used to interface the
[ ] Even bank memory [ ] Odd bank memory
[ ] I/O memory [ ] DMA

13. Consider the following set of 8085 instruction.

```
MVI A, 82H
ORA A
JP DSPLY
XRA A
DSPLY: OUT PORT1
HLT
```

The output at PORT1 is
[ ] 00H [ ] FFH [ ] 92H [ ] 11H

14. Which of the following is **NOT** a status flag in microprocessor?
[ ] Overflow flag [ ] Direction flag [ ] Interrupt flag [ ] Index flag

15. What is the content of accumulator of 8085 Microprocessor after the execution of XRI F0H instruction?
[ ] Complement the upper four bits of the accumulator in 8085
[ ] Complement the lower four bits of the accumulator in 8085
[ ] Clear the lower four bits of the accumulator in 8085
[ ] Clear the upper four bits of the accumulator in 8085

16. Which of the following is the addressing mode in which the memory location's effective address is written directly in the instruction?
[ ] Register addressing mode [ ] Register Indirect addressing mode
[ ] Based addressing mode [ ] Direct addressing mode

17. Regardless of the form of the primitive the actual _____ are determined solely by the contents of the SI, DI, DS and ES registers.
[ ] Opcodes [ ] Operands [ ] Memory modes [ ] Addressing modes

18. Which of the following are RESET signals of the 8085 processor?
[ ] S0, S1, IO/M [ ] RESET IN, RESET OUT
[ ] HOLD, HLDA [ ] READY, RD, WR, ALE

19. What does the last instruction of each subroutine that transfer the control to the instruction in the calling program with temporary address storage known as?
[ ] Call subroutine [ ] Return from subroutine
[ ] Branch to subroutine [ ] Jump to subroutine

20. The push and pop instructions belonging to the category of transfer instructions of microprocessor perform data transformation between _____.
[ ] Two registers [ ] Interface register and memory word
[ ] Processor register and interface register [ ] Processor register and memory stack

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F. M. : 40

SECTION "B"
[6Q. × 4 = 24 marks]

Attempt *ANY SIX* questions.

1. What is the difference between the Microprocessor and Microcontroller? Outline the functions of Bus Interface Unit (BIU) in 8086.

2. What is the process of DMA Transfer? Explain internal configuration of DMA Controller.

3. Briefly explain the functions of Memory Address Register, Memory Buffer Register, Instruction Register and Program Counter found in Microprocessor.

4. Explain the functional block diagram of 8085 Microprocessor. Define operation code and operands of 8085 Microprocessor.

5. What is the difference between interrupt service routine and subroutine? Explain stack overflow and underflow using assembly language.

6. Draw and describe pin diagram of 8288 Bus Controller.

7. What are the 8237 registers? Describe how the DMA can be implemented in 8086 processor?

SECTION "C"
[2Q. × 8 = 16 marks]

Attempt *ANY TWO* questions.

8. a. What do you mean by addressing mode? Explain the different addressing modes supported by 8086.

   b. Explicate the concept of segmented memory. What are its advantages?

9. Discuss internal configuration of 8259 Programmable Interrupt Controller. What are the steps of events observed in 8259?

10. Explain instruction cycle, machine cycle and T-states. Draw timing diagram of IN instruction with brief description. Differentiate between isolated I/O and memory mapped I/O.