KATHMANDU UNIVERSITY
End Semester Examination
August/September, 2017

SEP 0 4 2017

Level : B. E./ B. Sc.
Year : II
Time : 2 hrs. 30 mins.

Course : COMP 231
Semester : II
F. M. : 40

SECTION "B"

[6Q. × 4= 24 marks]

Attempt *ANY SIX*.

1. Define Microprocessor. Explain Harvard architecture. Differentiate it with Von Neumann architecture? [1+2+1]
2. What is bus buffering? Describe addressing modes of Intel 8085. [1+3]
3. Explain pin configuration of latches 8282 with figure.
4. What is machine cycle? Explain 8086 CPU registers. [1+3]
5. What are the applications of programmable interval timer 8254? Describe its modes with pulse diagram. [1+3]
6. Describe functional block diagram of 8288 bus controller with diagram.
7. What do you mean by parameter passing in stack? Illustrate with a programming. What are stack manipulation words? [1+2+1]

SECTION "C"

[2Q. × 8 = 16 marks]

Attempt *ANY TWO.*

8. Describe functional block diagram of Intel 8086 with figure. List the operating modes of 8086 microprocessor. [6+2]
9. What is interrupt? Explain the implications of programmable interrupt controller 8259A with its registers. What are the steps of events found in 8259A during data processing? [2+2+4]
10. Describe 8237 DMA Controller with pin diagram. Explain DMA transfer modes. [5+3]

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Mark Scored:

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Time: 30 min
F. M. : 10
Registration No.:
Date : SEP 0 4 2017

SECTION "A"
[20Q. × 0.5= 10 marks]

Tick [√] the most appropriate answer from the alternatives given. All symbols have their usual meanings.

1. In 8237, if each device is connected to a channel and is assigned to a fixed priority then it is said to be in _____.
   [ ] Rotating priority scheme
   [ ] Fixed priority scheme
   [ ] Rotating priority and fixed priority scheme
   [ ] Interrupt stage

2. The technique of assigning a memory address to each I/O device in the computer system is called:
   [ ] Memory-mapped I/O
   [ ] Ported I/O
   [ ] Dedicated I/O
   [ ] Wired I/O

3. Which of the followings are the three basic sections of a microprocessor unit?
   [ ] Operand, register, and arithmetic/logic unit (ALU)
   [ ] Control and timing, register, and arithmetic/logic unit (ALU)
   [ ] Control and timing, register, and memory
   [ ] Arithmetic/logic unit (ALU), memory, and input/output

4. Match the following

   a) MOV SB/SW
   b) CMPS
   c) SCAS
   d) LODS

   1) loads AL/AX register by content of a string
   2) moves a string of bytes stored in source to destination
   3) compares two strings of bytes or words whose length is stored in CX register
   4) scans a string of bytes or words

   [ ] a-3, b-4, c-2, d-1
   [ ] a-2, b-1, c-4, d-3
   [ ] a-2, b-3, c-1, d-4
   [ ] a-2, b-3, c-4, d-1

5. The register that stores all the interrupt requests in order to serve them one by one on priority basis is
   [ ] Interrupt Request Register
   [ ] In-Service Register
   [ ] Priority resolver
   [ ] Interrupt Mask Register

6. The number of PUSH instructions and POP instructions in a subroutine must be
   [ ] PUSH instructions must be greater than POP instructions
   [ ] POP instructions must be greater than PUSH instructions
   [ ] Both must be equal
   [ ] Instructions may be any kind

7. Which of the following command is used to make clear to all the internal registers of 8237?
[ ] Clear first/last flipflop
[ ] Clear mask register
[ ] Master clear command
[ ] Block transfer

8. The register that stores all the interrupt requests in it in order to serve them one by one on priority basis is
[ ] Interrupt Request Register
[ ] Priority resolver
[ ] In-Service Register
[ ] Interrupt Mask Register

9. What happened when the RET instruction at the end of subroutine is executed?
[ ] The information where the stack is initialized is transferred to the stack pointer
[ ] The memory address of the RET instruction is transferred to the program counter
[ ] Two data bytes stored in the top two locations of the stack are transferred to the program counter
[ ] Two data bytes stored in the top two locations of the stack are transferred to the stack pointer

10. 8086 is interfaced to two 8259s (Programmable Interval Timer).If 8259s are in master slave configuration, the number of interrupts available to the 8086 microprocessor is ____.
[ ] 8
[ ] 15
[ ] 16
[ ] 64

11. The TRAP is one of the interrupts available its INTEL 8085. Which one of the following statements is true of TRAP?
[ ] It is level triggered
[ ] It is negative edge triggered
[ ] It is positive edge triggered
[ ] It is both positive edge triggered and level triggered

12. While INX B instruction is executed
[ ] Only carry flag will be affected
[ ] Only carry and zero flags will be affected
[ ] All flags will be affected
[ ] No flags will be affected

13. Which statement is true for DMA?
[ ] DMA channel can be programmed to manually set up and start another DMA transfer
[ ] It allows certain hardware subsystems to read/write data to/from memory
[ ] 64 KByte section of memory address capability with multiple programming
[ ] Software instruction has different effect as the hardware reset

14. Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have
[ ] Interrupt handling ability
[ ] Multiple interrupt processing ability
[ ] Interrupt processing ability
[ ] Multiple interrupt executing ability

15. If 'n' denotes number of clock cycles and 'T' denotes period of the clock at which the microprocessor is running, then duration of execution of loop once can be denoted by
[ ] n+T
[ ] n*T
[ ] n-T
[ ] n/T

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16. In case of subroutines, the actual number of instructions executed by the processor depends on
[ ] Loop count
[ ] Length of procedure
[ ] Length of interrupt service routine
[ ] Bit size

17. In the instruction set,
MOV CX, BA03H
WAIT: DEC CX
NOP
JNZ WAIT
RET
if the zeroth condition is satisfied then, for execution, the JNZ instruction takes
[ ] 1 clock cycle
[ ] 3 clock cycles
[ ] 2 clock cycles
[ ] 4 clock cycles

18. In the application where all the interrupting devices are of equal priority, the mode used is
[ ] Automatic rotation
[ ] Specific rotation
[ ] Automatic EOI mode
[ ] EOI

19. The _____ can refer to either the time period during which one instruction is fetched from memory and executed when a computer receives a machine language instruction.
[ ] Instruction cycle
[ ] Memory data register
[ ] Instruction fetch operation
[ ] Instruction decoder

20. Consider the following set of 8085 instruction.
MVI A, 82H
ORA A
JP DSPLY
XRA A
DSPLY: OUT PORT1
HLT
What is the output of PORT1?
[ ] 00H
[ ] FFH
[ ] 92H
[ ] 11H