KATHMANDU UNIVERSITY
End Semester Examination
August/September, 2017

Mark Scored :

Level : B. E.
Year : II

Course : COMP 201
Semester : II

Exam Roll No. :

Time: 30 mins.

F. M. : 10

Registration No.:

Date SEP : 10 2017

SECTION "A"
[20 Q. × 0.5 = 10 marks]

Tick (√) the correct answer(s).

1. The largest integer that can be represented in 2's complement number using n bits is:
[ ] 2^n-1 [ ] 2^n [ ] 2^{n-1} -1 [ ] 2^{n-1}

2. The least negative value that the product of two 8 bits 2's complement number can take is:
[ ] -2^{14} [ ] -2^{15} [ ] -2^{10} [ ] -2^{12}

3. What the m-bit parallel adder consists of?
[ ] (m+1) full adders [ ] m/2 full adders
[ ] m-1 full adders [ ] m full adders

4. The register that keeps track of the instructions in the program stored in memory is _____
[ ] Accumulator [ ] Program counter
[ ] temporary register [ ] Instruction register

5. The device which is used to connect a peripheral to bus is called:
[ ] Control register [ ] Interface
[ ] Communication protocol [ ] decoder

6. Which shift is a shift micro operation which is used to shift a signed binary number to the left or right:
[ ] Logical [ ] Arithmetic [ ] Circular [ ] rotate

7. In a vectored interrupt_____
[ ] the branch address is assigned to a fixed location in memory.
[ ] the interrupting source supplies the branch information to the processor through an interrupt vector.
[ ] the branch address is obtained from a register in the processor
[ ] the branch address is not available

8. A stack organized computer use _____addressing.
[ ] indexed [ ] one [ ] two [ ] zero

9. If the value V(x) of the target operand is contained in the address field itself, the addressing mode is:
[ ] immediate [ ] direct [ ] indirect [ ] implied

10. What is the content of Stack Pointer (SP)?
[ ] Address of the current instruction [ ] Address of the next instruction
[ ] Address of the top element of the stack [ ] Size of the stack

11. In daisy chaining method of interrupt handing, how do devices are connected?
[ ] parallel [ ] random [ ] serial [ ] synchronous

12. In daisy chaining method device with PI=____and PO=_____is the one with higher priority that is requesting an interrupt.
[ ] 1, 0 [ ] 0, 1 [ ] 1, 1 [ ] 0, 0

13. The Excess-3 decimal code is a self-complementing code because:
(I) The binary sum of a code and its 9's complement is equal to 9.
(II) The binary sum of a code and its 10's complement is equal to 9.
(III) Complement can be generated by inverting each bit pattern.
[ ] I only [ ] I and II only [ ] I and III only [ ] II and III only

14. When an inverter is placed between both inputs of an SR flip flop, the resulting flip flop is:
[ ] JK flip flop [ ] D flip flop
[ ] T flip flop [ ] Master slave JK flip flop

15. In Branch and save return address (BSA) instruction, the RTL at the execution cycle at T4 is:
[ ] D_5T_4: DR←M [AR], AR←AR+1 [ ] D_5T_4: PC←AR, AR←AR+1
[ ] D_5T_4: M [AR] ←PC, AR←AR+1 [ ] D_5T_4: M [AR] ←AC, AR←AR+1

16. The infix expression (A* (B / C) + D) has reverse polish notation equivalent to:
[ ] A B C / * D + [ ] A B C * / D+ [ ] A B C / D * + [ ] A B C / D + *

17. In an unsigned multiplication algorithm, if the least significant bit of multiplier is 0, then what operation will you perform?
[ ] Addition [ ] Subtraction
[ ] Arithmetic shift right [ ] Logical shift right

18. In binary division the sign of the remainder is same as the sign of _____
[ ] quotient [ ] dividend [ ] divisor [ ] sequence counter

19. Cache memory works on the principle of:
[ ] Locality of data [ ] Locality of reference
[ ] Locality of memory [ ] Locality of reference & memory

20. When the control function $\mathbf{D_7IT_3 = 1}$, which operation will be executed by the basic computer?
[ ] Execute register-reference instruction [ ] AR ← M [AR]
[ ] Execute input-output instruction [ ] Nothing