KATHMANDU UNIVERSITY
End Semester Examination [C]
April, 2023

Score:

Level : B.E.
Year : IV

Course : COEG 401
Semester : I

Exam Roll No:

Time: 30 mins.

F.M. : 10

06 APR 2023

Registration No.:

Date :

SECTION "A"
[20 Q. × 0.5 = 10 marks]

Encircle the most appropriate option or write down the appropriate answer.

1. Which of the following systems is controllable?
   a. A system with more inputs than outputs.
   b. A system with more outputs than inputs.
   c. A system with an equal number of inputs and outputs.
   d. A system with non-linear dynamics.

2. The transfer function of the following system is _____.

$$\dot{\underline{x}} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \underline{x} + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} u \qquad y = \begin{bmatrix} 0 & 0 & 0.5 \end{bmatrix} \underline{x}$$

   a. $G(s) = \frac{s}{s+1}$ b. $G(s) = \frac{1}{2s}$ c. $G(s) = \frac{2}{s}$ d. $G(s) = \frac{1}{6s+1}$

3. A mathematical model of a system can be used to observe _____.
   a. transient response
   b. steady state response
   c. both transient and steady state response
   d. neither transient nor steady state response

4. In a digital control scheme, selection of large sampling interval _____.
   a. does not contribute on steady state performance
   b. deteriorates the steady state performance
   c. highly effect system's steady state performance
   d. influences steady state performance that depends on plant parameters

5. The state space representation of a system is _____.
   a. unique b. not unique
   c. unique if minimal d. unique for given mathematical model

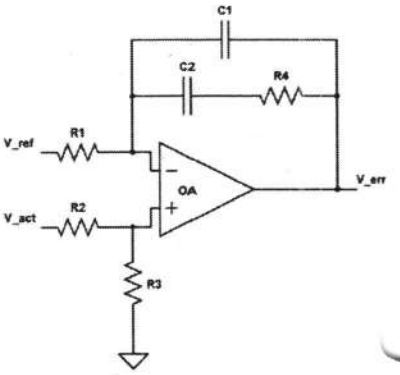
6. The mathematical model of the equation $G(s) = \frac{s+0.01}{s^2+2}$ has ____ differential equations.
   a. 1 b. 2 c. 3 d. 4

7. For a fifth order system to be strictly proper, number of zeros should be _____.
   a. >4 b. >5 c. <5 d. =5

8. Observable form of state space realization of a non-minimal transfer function is _____.
   a. controllable and observable
   b. controllable but not observable
   c. observable but not controllable
   d. neither controllable nor observable

9. The condition of several boards trying to be bus master at the same time, creating a conflicting situation, is called _____.
   a. bus arbitration
   b. bus contention
   c. block transfer
   d. none of these

10. Which controller is implemented in the given figure?
   a. P Controller
   b. PD Controller
   c. PI Controller
   d. PID Controller



11. If PI controller is implemented in forward part of a closed loop system, the rise time is _____ and steady state error is _____.
   a. decreased, unchanged
   b. unchanged, decreased
   c. decreased, decreased
   d. increased, decreased

12. Which of the following is **TRUE** for derivative control?
   a. Decrease overshoot and increase steady state error.
   b. Decrease both overshot and settling time.
   c. Increase both overshoot and settling time.
   d. Increase overshoot and decrease settling time.

13. Zero state response of a system results only form the _____.
   a. internal disturbance
   b. external input
   c. feedback
   d. driving input

14. Which of the following is **NOT TRUE** for resource sharing and task allocation?
   a. In a multitasking environment with one processor, more than one task can run in CPU.
   b. In static priority allocation, the low priority tasks may not execute at all.
   c. Shared resources are accessed in Critical Region of the code.
   d. Use of static priority allocation can bring deadlock in the system.

15. Which of the following instructions of PLC operates with content of stack?
   a. AND
   b. ORB
   c. ANI
   d. OR

16. In real time control system _____.
   a. system never reaches deadlock condition
   b. task priority is either fixed or determined by the operating system
   c. multi-tasking is not possible
   d. only event-based interrupts are used

17. When some or all processes in a system are halted waiting for something to happen, then the system is in _____.
   a. ISR
   b. starvation
   c. deadlock
   d. race condition

18. To avoid integral windup, integral part is adjusted by limiting _____.
    a. Reference b. error c. output d. control signal

19. Which of the following is **TRUE** for ballast coding?
    a. Interrupt cannot be used
    b. Independent of CPU clock rate
    c. CPU is never kept busy
    d. Execution time of the code is not considered

20. Write down assembly code for following ladder logic.