KATHMANDU UNIVERSITY
Second Internal

Level: UNG/CE	**Course: EEEG 211**	**F.M.: 16**
Year: II	**Time: 1 Hrs.**	**Semester: I**

Attempt any 4 Question. [4 x 4 = 16]

1. Design a **voltage-divider** bias network using a BJT having a gain of -15V/V.
   Hint: Use V_{cc} = 10V, I_E = 1 mA, V_{CE} = ½ V_{CC}.
2. Sketch the **transfer characteristics** of an N-channel depletion-type MOSFET with I_{DSS}=12 **mA** and V_P = -8V for a range of V_{GS} = - V_P to V_{GS} =1 V. Explain the construction and working principle of **JFET**.
3. For the network of figure 1. Determine:
   a. I_B b. I_C c. V_E d. V_{CE}

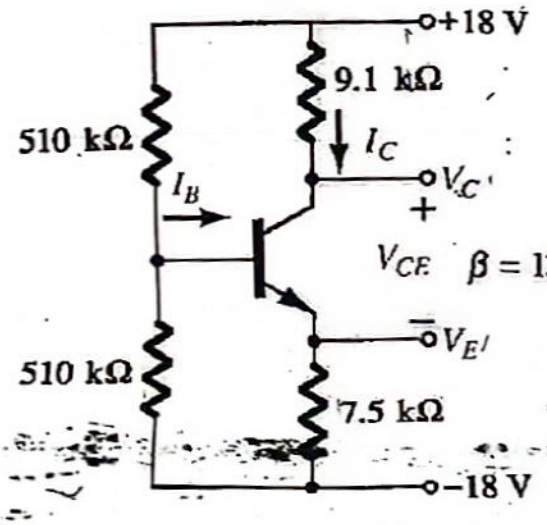

Figure 1

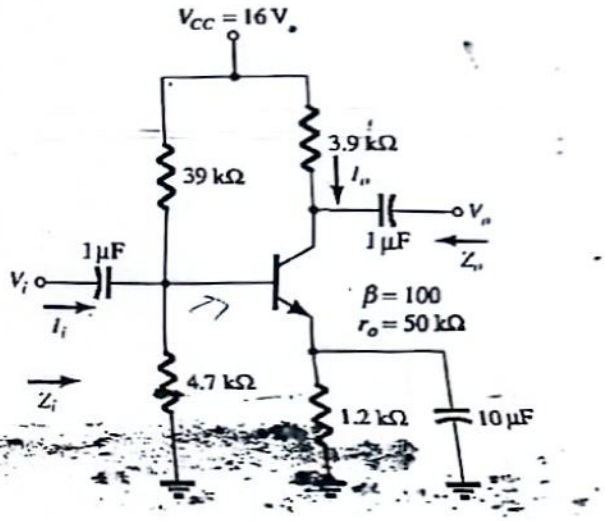

Figure 2

4. Design an **emitter-stabilized** bias network at $I_C = \frac{1}{2} I_{C\,sat}$ and $V_{CE} = \frac{1}{2} V_{CC}$. Use $V_{CC} = 20V$, $I_{Csat} = 10\ mA$, β= 120, and $R_C = 4\,R_E$.
5. For the network of **figure 2**.
   a. Calculate I_B and I_C.
   b. Determine r_e.
   c. Determine Z_i and Z_O.
   d. Find A_V.