KATHMANDU UNIVERSITY
First Internal Examination
2025

Level: BE
Year: II
Time : 50 min

Course: EEEG202
Semester: I
F.M. : 15

Figure in the margin indicates the full mark. Students are required to answer in their own words as far as practicable.

1. Design a combinational logic circuit for carry lookahead generator for 4-bit parallel adder. [4]
2. Write the truth table and design logic circuit for 3bit binary to gray code converter. [3]
3. Design a logic circuit for a lamp controlled by four switches A, B, C and D. The conditions for lamp to glow are: Switch 2 closed or switch 2 and 3 closed or all switch are closed. Implement the logic circuit using NAND gates only. [4]
4. Simplify the following Boolean expression using K-map: [4]
   $F(w,x,y,z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$

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